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Comprehensive behavioral model of dual-gate high voltage JFET and pinch resistor

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ABSTRACT

Many analog technologies operate in large voltage range and therefore include at least one or more high voltage devices built from low doped layers. Such devices exhibit effects not covered by standard compact models, namely pinching (depletion) effects, in high voltage FETs often called quasisaturation. For example, the conventional compact JFET model is insufficient and oversimplified. Its scalability is controlled by the area factor, which only multiplies currents and capacitances but does not take into account existing 3-D effects. Also the optional second independent gate is missing. Therefore, the customized four terminal (4T) model written in Verilog-A (FitzPatrick and Miller, 2007; Sagdeo, 2007) was developed. It converges very well, its simulation speed is comparable with conventional compact models, and contains all required phenomena, including parasitic effects as, for example, impact ionization. This model has universal usage for many types of devices in various high voltage technologies such as stand-alone voltage dependent resistor, pinch resistor, drift area of power FET, part of special high side or start-up devices, and dual-gate JFET.

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1. Introduction

Modeling work on JFETs has been mainly focused on three-terminal JFETs [3,4]. This paper introduces the comprehensive model enabling using two independent gates, one top-side, one bottom-side, and their mutual interaction. Most existing publications about (dual-gate) JFET model are focused on DC parameters [5–7]. Recently published dual-gate JFET [5] provides more physical and less empirical solution and their DC model can be in many cases more accurate. However, in dual-gate JFET the top-side gate not necessarily covers the whole JFET channel, as demonstrated in Fig. 8. The ratio of covered and uncovered channel controls the dependency of pinch-off on V_{DS}. In this paper this dependency is modeled by the empirical equation. Next merit of the presented model is the addition of impact ionization to the leakage current of both gates. In presented model the capacitance parameters were implemented by using the structural model defined by instantiation of Verilog-A [1,2] component with the implementation of additional voltage dependency. For the next model version it is planned to switch to the charge controlled model as recommended in [8].

The presented Verilog-A model is relatively complex, containing DC parameters, capacitance parameters, parasitic parameters for leakage current and impact ionization, temperature parameters and statistical parameters. It does not yet cover the self-heating and noise parameters [4].

The model was extended for use in various applications, e.g., high voltage LDMOS drift area in combination with PSP [9], HiSIM [10] or BSIM4 [11] compact MOSFET models. Another application where the model can be used is the pinch resistor, where using the conventional compact JFET model is insufficient. The model can be also applied to the dual-gate JFET (high voltage JFET with two independent gates). The dual-gate JFET is a device not supported by the compact SPICE models, although several important applications exist [12].

The following text demonstrates the evolution of the model and its application in various high voltage devices, namely the pinch resistor and the dual-gate JFET, where each of them requires a different concept. For example, the lateral pinching is important for the pinch resistor and therefore the pinch-off is width-dependent, while this effect is negligible for the oval-shape high voltage JFET. On the other hand, as depicted in Fig. 8, the high voltage JFET mentioned below has two independent gates (substrate

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from the bottom and P implant from the top) which requires an implementation of their interaction to the model.

2. DC model

2.1. Customized compact JFET model

Let's start with the 3-terminal JFET modeled by Shichman–Hodges model for linear region ($0 < V_{DS} < (V_{GS} - V_{th})$). The current flowing from drain to source is defined as [13]

$$I_{DS} = \beta V_{DS}(1 + \lambda V_{DS})(2(V_{GS} - V_{th}) - V_{DS}) \quad (1)$$

where β is the transconductance parameter, λ is velocity overshoot coefficient, and V_{th} is threshold (pinch-off) voltage.

For the size dependency evaluation let's consider JFET in linear region where V_{GS} and V_{DS} are very close to 0 volts. The resistance of JFET is then defined as

$$R = \frac{V_{DS}}{I_{DS}} = \frac{1}{-2\beta V_{th}} = R_{SH}\frac{L + \Delta_L}{W + \Delta_W} \quad (2)$$

where R_{SH} is the sheet resistance, Δ_L is length offset and Δ_W is width offset. The transconductance parameter can then be expressed as

$$\beta = -\frac{1}{2V_{th}R} = -\frac{1}{2V_{th}R_{SH}\frac{L+\Delta_L}{W+\Delta_W}} \quad (3)$$

Substituting (3) in (1) the JFET model becomes scalable with the resistor length and width and suitable for modeling voltage-dependent resistors.

The next phenomenon which has to be taken into account is the impact of a lateral pinching and its width dependency. The voltage dependent resistor is typically pinched from 3 sides: bottom, right and left. For very wide shallow resistors, bottom pinching dominates, while narrow deep resistors are dominated by right and left pinching. This effect is modeled by the parametrization of JFET parameter V_{th} as described in the following equation

$$V_{th} = \frac{V_{thinf}}{1 + \frac{2x_j}{W}} \quad (4)$$

where V_{thinf} is the threshold (pinch-off) voltage for infinitely wide resistor and x_j is resistor depth. The model is sufficient for most voltage dependent diffusion or implant resistors, but its use for the real pinch resistor, operating in the saturation region, is limited.

2.2. Behavioral JFET model – first prototype

Therefore a behavioral pinch resistor model was developed based on the following physical elements: vertical and lateral built-in potentials [3]

$$\psi_v = \frac{k_b T}{q}\ln\frac{N_{body}N_{tub}}{n_i^2} \quad (5)$$

$$\psi_l = \frac{k_b T}{q}\ln\frac{N_{side}N_{tub}}{n_i^2} \quad (6)$$

and vertical and lateral pinching factors [3]

$$\alpha_v = \sqrt{2\epsilon_0\epsilon_r\frac{N_{tub}}{qN_{body}(N_{body} + N_{tub})}} \quad (7)$$

$$\alpha_l = \sqrt{2\epsilon_0\epsilon_r\frac{N_{tub}}{qN_{side}(N_{side} + N_{tub})}} \quad (8)$$

where k_b is Boltzmann constant, T is absolute temperature, q is elementary charge, n_i is intrinsic carrier concentration of used material, ϵ_0 is vacuum permittivity, ϵ_r is permittivity of used material, and $N_{body}, N_{side}, N_{tub}$ are tuning parameters described in Table 1. The total current between drain and source derived from [3] is

$$I_{res} = \frac{V_{DG} - V_{SG}}{r_{ho}(L + \Delta_L)}(1 + \lambda V_{DS}) \times \left(W - 2\alpha_l\sqrt{\psi_l + \frac{V_{DG} + V_{SG}}{2}} + \Delta_W\right) \times \left(x_j - \alpha_v\sqrt{\psi_v + \frac{V_{DG} + V_{SG}}{2}}\right) \quad (9)$$

where r_{ho} is tuning parameter described in Table 1. The original equation of I_{res} in [3] contains additional effect of top pinching caused by metal plate above field oxide. However, this effect does not exist in devices described below and it is not considered here.

The saturation of current I_{res} is handled by setting the derivative of (9) with respect to V_{DG} equal to zero, which expresses saturation voltage V_{DGsat}. The applied V_{DG} and V_{DGsat} are then fed into a conventional saturation smoothing function, resulting in an effective bias V_{DGeff} [3], substituted for V_{DG} in (9). However, the solution could not be obtained explicitly, therefore it was iteratively solved by the simulator during simulation using a dedicated circuit containing arbitrary sources.

Although the smooth and continuous transition from the linear region into saturation region was ensured, the simulation time was relatively long and in some cases even the convergence issues appeared. Therefore some improvements were introduced.

2.3. DC model of pinch resistor

First of all, the pinch resistor has no top pinching caused by the metal/poly flap, described in [3]. The top and bottom pinching have both the same physical basis, only the gate concentration is different. However, the top gate is shorted to the substrate, as illustrated in Fig. 2. We can thus consider only one pinching gate, which simplifies (9) and enables us to express the explicit solution of V_{DGeff} and V_{SGeff}. This significantly improves model convergence and simulation speed. Thus, no recursive function is required in the model any more.

The next step was linearization of the model close to $V_{DS} = 0$ V, where a too complicated calculation of the current caused the convergence issues. Therefore the model was divided into three operation areas.

For $V_{DS} > 1$ nV:

$$I_{res} = \frac{V_{DSeff}}{r_{ho}(L + \Delta_L)}(1 + \lambda V_{DS}) \times \left(W + \Delta_W - GMOD \times 2\alpha_l\sqrt{\psi_l + \frac{V_{DSeff} + r_{sub}V_{SG}}{2}}\right) \times \left(x_j - \alpha_v\sqrt{\psi_v + \frac{V_{DSeff} + r_{sub}V_{SG}}{2}}\right) \quad (10)$$

Table 1
DC parameters of JFET.

Parameter	Description	Unit
N_{body}	JFET body (drift area) concentration	$1/cm^3$
N_{side}	Side concentration of JFET body	$1/cm^3$
N_{tub}	Gate (substrate) concentration	$1/cm^3$
x_j	JFET depth	μm
λ	Velocity overshoot coefficient	1/V
r_{ho}	Channel resistivity in ON state	$\Omega/\mu m^2$
Δ_L	Length offset	μm
Δ_W	Width offset	μm

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