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Half-Corbino short-channel amorphous In–Ga–Zn–O thin-film transistors with a-SiO_x or a-SiO_x/a-SiN_x passivation layers

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ABSTRACT

We investigated the electrical properties and stability of short-channel half-Corbino amorphous In–Ga–Zn–O (a-IGZO) thin-film transistors (TFTs). In the linear region, the fabricated half-Corbino a-IGZO TFT with a channel length of 4.5 μm achieves a geometrical factor (f_g) of ~2.7, a threshold voltage (V_T) of ~2.4 V, a field-effect mobility (μ_{eff}) of ~15 cm^2/Vs, a subthreshold swing (*SS*) of ~320 mV/dec and an off-current (I_{OFF}) < 10^{-13} A. In the saturation region, asymmetric electrical characteristics such as drain current were observed under different drain bias conditions. The electrical properties asymmetry of half-Corbino a-IGZO TFTs was explained by various geometrical factors owing to the short-channel effect. The reduced V_T and increased *SS* at V_{DS} = 15 V is explained by the drain-induced Schottky barrier lowering. In addition, the bias-temperature stress (BTS) was performed for half-Corbino a-IGZO TFTs with both amorphous silicon oxide (a-SiO_x) single layer and a-SiO_x/amorphous silicon nitride (a-SiN_x) bilayer passivation (PV) structures. The device with bilayer PV shows a threshold voltage shift (ΔV_T) of +2.07 and −0.5 V under positive (PBTS = +15 V) and negative BTS (NBTS = −15 V) at 70 °C for 10 ks, respectively. The origins of ΔV_T during PBTS and NBTS for half-Corbino a-IGZO TFTs with single and bilayer PV structures were studied. To improve the device electrical stability, the bilayer PV structure should be used.

1. Introduction

The Corbino (annular) source/drain (S/D) geometry has been developed for various semiconductor technologies [1–3]. Previously, we reported both full-Corbino and half-Corbino hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) and investigated their asymmetric electrical properties under different drain bias conditions [4–6]. To explain the asymmetric electrical behaviors of Corbino a-Si:H TFTs, geometrical factors (f_g) were developed under different drain bias conditions [4]. We demonstrated that both full or half-Corbino a-Si:H TFTs are suitable as the switching transistor for active-matrix liquid crystal displays (AM-LCDs) to reduce the gate-to-source parasitic capacitance (C_{GS}) and the pixel error voltage [5]. Besides, half-Corbino a-Si:H TFTs can also be employed for active-matrix organic light emitting displays (AM-OLEDs) as the driving transistors to reduce the DC bias on the driving transistor and thus minimize the display power consumption [5,6]. However, a low field-effect mobility (μ_{eff}) of a-Si:H TFTs (<1 cm^2/Vs) limits their applications in ultra-high resolution, large area active-matrix flat-panel displays (AM-FPDs). Among the candidates of high-mobility TFT technologies, amorphous In–Ga–Zn–O (a-IGZO) TFTs are widely considered as the next generation TFT technology for AM-FPDs due to their high field-effect mobility (μ_{eff} > 10 cm^2/Vs), low leakage current (I_{OFF} < 10^{-13} A), improved electrical stability and high spatial uniformity [7,8]. Mativenga et al. reported a full-Corbino a-IGZO TFT as the driving TFT for large area AM-OLEDs [9,10]. This study shows that a uniform organic light emitting diode (OLED) current under various bias voltages can be achieved due to a large output resistance (R_{OUT}), when the outer-drain bias condition is used. However, the full-Corbino a-IGZO TFT structure usually takes a larger pixel area, which is not ideal for ultra-high resolution displays. It also requires separated deposition and patterning steps for the outer and inner electrodes, i.e. the inner electrode has to be deposited and patterned after device passivation (PV) [9,10].

In this paper, for the first time, we reported half-Corbino a-IGZO TFTs and investigated their asymmetric electrical properties. Asymmetric geometrical factors under different drain bias conditions were developed. The source/drain (S/D) contact quality was studied using a Schottky metal–semiconductor–metal (MSM) contact model. It is also critical to evaluate and optimize the device electrical stability of half-Corbino a-IGZO TFTs for display and detector applications. Since the device electrical instability can

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be influenced by the PV structures, we also investigated the electrical properties after bias-temperature stress (BTS) for TFTs with amorphous silicon oxide (a-SiO_x) single layer and a-SiO_x/amorphous silicon nitride (a-SiN_x) bilayer PV structures. The physical origins of device electrical instability were carefully studied.

2. Device fabrication

The half-Corbino TFT was fabricated using a six photo-masks process procedure. First, an amorphous silicon oxide (a-SiO_x) buffer layer was deposited on a glass substrate using plasma-enhanced chemical vapor deposition (PECVD). The molybdenum (Mo) bottom gate was DC sputtered and patterned (Mask #1). PECVD was used to grow the a-SiO_x gate insulator (200 nm). Then a 50 nm a-IGZO channel film was DC sputtered; the active island was patterned by wet etching (Mask #2). To protect the a-IGZO channel, an a-SiO_x etch stopper layer (ESL) was deposited using PECVD. The ESL was patterned by a reactive ion etching (RIE) method (Mask #3). The gate via was formed using another mask (Mask #4). The 200 nm Mo source, drain and gate electrodes were DC sputtered and etched (Mask #5). Then the first anneal was performed. The entire device was passivated using either PECVD a-SiO_x (300 nm) single layer or a-SiO_x/amorphous silicon nitride (a-SiN_x) (150 nm/150 nm) bilayer structures. It is known that a-SiN_x has a better protection against outside environment, such as moisture. Therefore, double layers will be a preferred passivation design. It should be noted that hydrogen (H) can be introduced to both a-SiO_x and a-SiN_x layers during PECVD process. In general, the H content in a-SiN_x is higher than in a-SiO_x. The typical mechanical stress for a-SiO_x is −250 MPa (compressive) and for a-SiN_x is 150 MPa (tensile). After the PV, source/drain (S/D) contact vias were developed (Mask #6). Finally, the second anneal was performed. Both thermal anneals were one hour long and controlled to be no more than 300 °C.

Fig. 1 shows the top view (a) and cross-sectional view (b) of the half-Corbino a-IGZO TFT. The half-Corbino a-IGZO TFT consists of a rod-shaped inner electrode and a half-ring shaped outer electrode. The radius of the inner electrode (R_1) and outer electrode (R_2) were measured to be 2.0 and 6.5 μm, respectively. The channel length (L) is 4.5 μm. Two drain-bias conditions can be used: (1) "inner-drain", where the rod-shaped inner electrode and the half-ring shaped outer electrode are biased as the drain and source, respectively; and (2) "outer-drain" (the opposite bias condition).

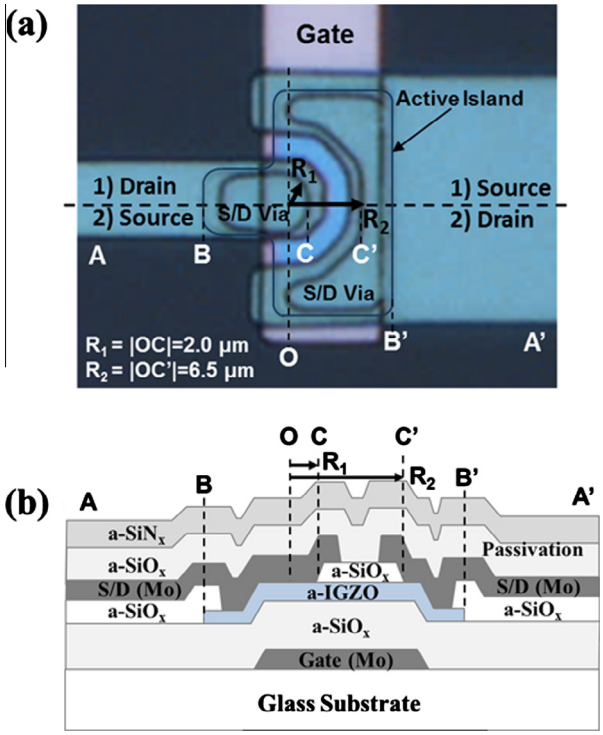

Fig. 1. (a) Top view and (b) cross-sectional view of the half-Corbino a-IGZO TFT (R_2/R_1 = 6.5 μm/2 μm) with a-SiO_x/a-SiN_x bilayer PV.

3. Results and discussion

3.1. Electrical properties of the short-channel half-Corbino a-IGZO TFT

The transfer (Fig. 2) and output characteristics (Fig. 3) of the half-Corbino a-IGZO TFT were measured under both (1) inner-drain and (2) outer-drain bias conditions. Asymmetric electrical properties under different drain bias conditions can be observed at a large drain-to-source voltage (V_{DS}). The inner-drain bias condition achieves greater drain current (I_D) in comparison with the outer-drain bias condition in the saturation region. It is obvious that the output characteristics, especially the inner-drain bias condition, do not saturate at V_{GS} = 15 V. The unsaturated output characteristics clearly indicate the existence of short-channel effect in half-Corbino TFTs. However, the I_D difference in the linear region (V_{DS} < 2.5 V) for two bias conditions is negligible as shown in the zoom-in output characteristics (Fig. 4). The experimental results are consistent with our previous observations for full and half-Corbino a-Si:H TFTs [4–6].

The source/drain (S/D) contacts quality of the half-Corbino a-IGZO TFT is evaluated by taking the derivative of I_D–V_{DS} curves ($\partial I_D/\partial V_{DS}$) in the linear region ($V_{DS}$ < 2.5 V). The result shows that the S/D contacts are not ideal ohmic, since $\partial I_D/\partial V_{DS}$ is decreasing with V_{DS}, which is consistent with our previous finding [11]. We

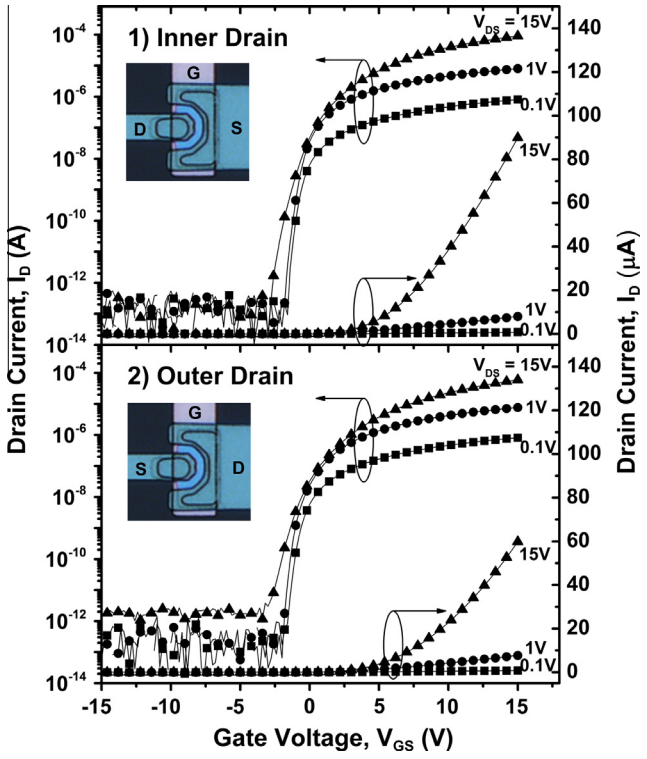

Fig. 2. Transfer characteristics of the half-Corbino a-IGZO TFT (R_2/R_1 = 6.5 μm/2 μm) with a-SiO_x/a-SiN_x bilayer PV under (1) inner drain and (2) outer drain bias conditions.