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Physically-based simulation of zinc oxide thin-film transistors: Contact resistance contribution on density of states

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ABSTRACT

In this work, using a physically-based simulator, the density of states DOS is modeled to reproduce the experimental electrical characteristics of ZnO TFTs fabricated by Ultrasonic Spray Pyrolysis at 200 °C. The contact resistance was experimentally extracted from the ZnO TFTs and included into the simulation, in order to separate the metal–semiconductor interface contribution from the DOS. A comparison between the modeled DOS considering the contact resistance and disregarding it is also presented. It is proposed to consider the acceptor-like states and the tail-donor states, where the deep-acceptor states have approximately an exponential form and the distribution of tail-acceptor states are sharper than the distribution of tail-donor states. The simulated electrical characteristics reproduce very well the experimental data at different channel lengths. The use of physically-based simulation can be useful to model the DOS of Oxide semiconductor films in TFTs by reproducing the experimental data.

1. Introduction

Currently, oxide semiconductors have a wide application in Thin-film Transistors (TFTs) to enable low-cost electronics that replace the mature a-Si TFT Technology [1]. One of the bottlenecks in oxide TFT technologies is the material science and modeling of the devices. Since to modeling the electrical performance of the devices, it is necessary to know the approximated distribution of defects in the gap of the semiconductor (active layer), typically the so-called density of states (DOS) [2–5]. First of all, the material science in oxide semiconductors is still not completely understood. The role of impurities and defects distribution in electronic properties of most oxide semiconductors is still controversial [5–7]. Second of all, the calculation of the DOS in semiconductors materials is a complex work, since the extracted DOS reflects contributions of the main interfaces in the TFTs (metal–semiconductor and insulator–semiconductor). Typically, in order to extract a realistic DOS, the TFTs need to be free of parasitic effects related to low-quality interfaces (high contact resistance, gate leakage current effects, etc.) [2–4]. However, usually, having a metal-oxide semiconductor contact without interface states is difficult. Also, matching the semiconductor and metal work functions is nearly impossible [6]. It is important to say that the contact metallization technology in oxide semiconductors has not been explored extensively [6]. Finally, it is assumed that the DOS is homogenous throughout the active layer, there are no surface states and the DOS is constant through the time, however, in reality these are not true, making even more complex the DOS calculation [2–4]. Some methods have been reported to extract approximately the DOS, however, they require complex calculations or may introduce changes in the electrical characteristics of the Oxide TFTs. Also, they do not consider the contact resistance contribution on the DOS [5,8–14]. It is well-known, the contact resistance reduces the on-current, affects the off-current, the on/off-current ratio and masks the real value of the extracted electron mobility. Moreover, even some authors have reported higher values of subthreshold slope and a reduction in transconductance due to a high contact resistance [15–18]. Since the DOS is calculated from the electrical characteristics of the TFTs, for the above reasons, easily one can attribute some of the contact resistance effects to the DOS, resulting in an inaccurate modeled DOS and hence, an inaccurate modeled device.

The advantage of using physically-based simulators is that they provide information that is difficult or impossible to measure. Moreover, one can incorporate the necessary parameters in order to enable (simulate) the contribution of the different interfaces in the device (fixed oxide charge density, interface charge density, high contact resistance, etc.). The drawbacks of physically-based simulation are that it is necessary to know the relevant material parameters and device physics to be incorporated into the simulator, as well, numerical procedures must be implemented to solve the associated equations.

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In this work, we propose an approximation of the DOS for the ZnO TFTs fabricated by Ultrasonic Spray Pyrolysis at 200 °C, then using a physically-based simulator (Silvaco) the DOS is modeled to reproduce the experimental electrical characteristics of the devices. Also, the contact resistance was experimentally extracted from the ZnO TFTs and included into the simulation, in order to separate the contact resistance contribution from the DOS. A comparison between the modeled DOS considering the contact resistance and disregarding it is also presented.

2. Experiment

The ZnO films were deposited using a typical home-made ultrasonic spray pyrolysis deposition system adapted from an ultrasonic humidifier (Heaven Fresh), from 0.2 M precursor solution of Zinc acetate in methanol, using air as carrier gas at flow rate of 467 sccm. During deposition the substrate was placed on a hotplate at 200 °C. The fabrication procedure of the inverted coplanar ZnO TFTs (bottom-contact bottom-gate) can be found elsewhere [19]. The electrical characteristics were measured using the Keithley-4200 Semiconductor Characterization System under dark conditions, room temperature and air ambient. The transfer characteristics were measured both forward and reverse sweep. The averages of the curves were obtained to extract the device parameters. The average values extracted were affected approximately ±15% of its value by the hysteresis.

The simulations were done as follows: using ATHENA, the TFT structures were generated following the fabrication process established. Si_3N_4 was defined as the substrate, with no physical effects on the results. The gate insulator used in the simulations was silicon oxide with default properties values. The thickness used for the silicon oxide and ZnO films were 50 nm and 35 nm, respectively. The thickness of the source and drain Aluminum electrodes were 100 nm. After that, using ATLAS, the transfer characteristics were simulated. For the simulation, the TFT module was used. Ohmic contacts were used and the temperature was set at 300 K. Newton's method was the numerical method used for equations solution. Discrete trap energy levels were considered for the simulations. The results presented are representative of simulated and experimental devices with channel lengths L from 10 to 65 μm, where similar behavior was obtained. The channel width W of experimental TFTs were 120 μm.

3. Results and discussion

In order to obtain a more accurate DOS, it is recommended to separate the contribution of the interfaces (metal–semiconductor and insulator–semiconductor) as much as possible. Therefore, one must extract experimentally the main device parameters and include them into the simulation. Fig. 1 shows the normalized transfer characteristics of ZnO TFTs with different channel lengths. As can be seen, there is no appreciation of short-channel effects in the electrical characteristics [18]. In this way, is easier to compare the fit of the experimental and simulated electrical characteristics of the TFTs at different channel lengths.

The electron field-effect mobility and threshold voltage were extracted from the square root of Ids versus Vgs, using the Eq. (1) of the TFTs in the saturation regime (Vds = 25 V) [20], where the values obtained are shown in Fig. 2.

$$\mathrm{Ids} = \mu_{\mathrm{FE}} \cdot C_{\mathrm{ox}}(W/2L)(\mathrm{Vgs} - V_{\mathrm{T}})^2 \quad (1)$$

where μ_{FE} is the field-effect mobility, C_{ox} is the capacitance per unit area of the gate insulator, W and L are the channel width and the length, respectively, and V_{T} is the threshold voltage.

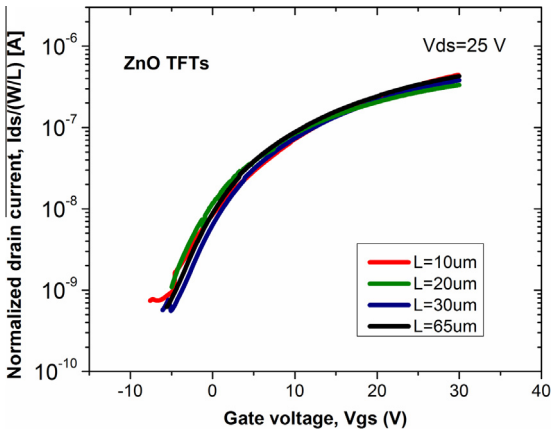

Fig. 1. Normalized transfer characteristics of ZnO TFTs with different channel lengths.

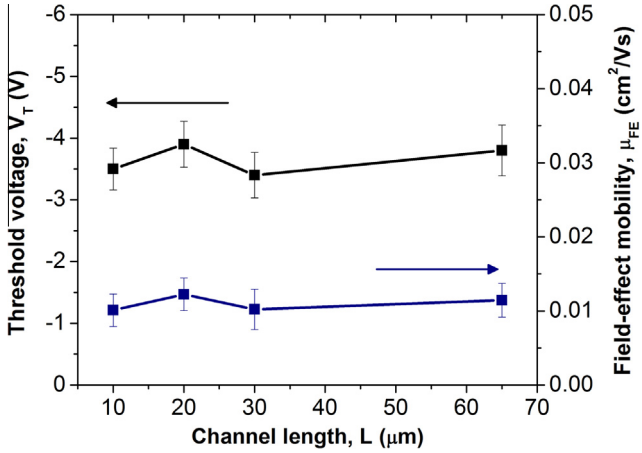

Fig. 2. Threshold voltage and field-effect mobility experimentally extracted as function of channel length.

Typically, in the ZnO TFTs, the subthreshold slope is dependent on the trap density in the active layer ZnO (N_{T}) and at the SiO_2/ZnO interface (D_{it}). The subthreshold slope can be approximated as the following equation [20]:

$$\mathrm{SS} = \mathrm{qK_B}T(N_{\mathrm{T}}T_{\mathrm{ZnO}} + D_{\mathrm{it}})/C_{\mathrm{ox}}\log(e) \quad (2)$$

where q is the electron charge, K_{B} is the Boltzmann constant, T is the absolute temperature, T_{ZnO} is the ZnO thickness and C_{ox} is the capacitance per unit area of the gate insulator. If N_{T} or D_{it} is separately set to zero, the respective maximum values of N_{T} and D_{it} are obtained. The N_{T} and D_{it} values for ZnO TFTs were $7.8 \times 10^{18}\ \mathrm{cm^{-3}\ eV^{-1}}$ and $2.7 \times 10^{13}\ \mathrm{cm^{-2}\ eV^{-1}}$, respectively. These values are higher than the typically reported for ZnO TFTs [9,21,22]. Therefore, it is expected that the final DOS be higher than the reported by other authors.

Moreover, in order to separate the metal–semiconductor interface contribution from the DOS, the contact resistance was extracted from the ZnO TFTs and included into the simulation. A high contact resistance was confirmed by the extrapolation of the width-normalized contact resistance (RcW) (obtained from the linear region of Ids vs Vds) for different channel lengths and gate voltages Vgs [23]. The 2RcW obtained was approximately 2800 Ω cm, this value is similar to the extracted previously in Al–ZnO contacts by Transmission Line Method [19]. The contact resistance introduced into the simulator was 875 Ω cm for each