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Fabrication and electrical characterization of homo- and hetero-structure Si/SiGe nanowire Tunnel Field Effect Transistor grown by vapor–liquid–solid mechanism

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A B S T R A C T

We demonstrate the fabrication and electrical characterization of Ω-gate Tunnel Field Effect Transistors (TFET) based on p-Si/i-Si/$n^{+}Si_{0.7}Ge_{0.3}$ heterostructure nanowires grown by Chemical Vapor Deposition (CVD) using the vapor–liquid–solid (VLS) mechanism. The electrical performances of the p-Si/i-Si/$n^{+}Si_{0.7}Ge_{0.3}$ heterostructure TFET device are presented and compared to Si and $Si_{0.7}Ge_{0.3}$ homostructure nanowire TFETs. We observe an improvement of the electrical performances of TFET with p-Si/i-Si/$n^{+}Si_{0.7}Ge_{0.3}$ heterostructure nanowire (HT NW). The optimized devices present an Ion current of about 245 nA at V_{DS} = −0.5 V and V_{GS} = −3 V with a subthreshold swing around 135 mV/dec. Finally, we show that the electrical results are in good agreement with numerical simulation using Kane's Band-to-Band Tunneling model.

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1. Introduction

The power dissipation associated with a high off-state current (Ioff) is one of the major problem to the further scaling of CMOS devices. In order to decrease the Ioff and the voltage supply (V_{DD}), it will be necessary to reduce the subthreshold swing (SS) [1]. In fact, the conventional MOSFET has a physical limit of SS (60 mV/dec at 300 K) due to the thermionic conduction mechanism. To reduce the SS and the Ioff, various carrier injection mechanisms have been proposed [2–4]. One of the most promising for low energy consumption device is the Tunnel FET to achieve steep SS, low Ioff current and high Ion/Ioff ratio at very low V_{DD}. The TFET consists of a gated p-i-n diode operated in reverse bias whose carrier transport is principally governed by band-to-band tunneling (BBT) of carriers through the forbidden band gap. Tunnel FET current (Eq. (1)) is proportional to BBT transmission which is calculated using the Wentzel–Kramers–Brillouin (WKB) approximation [5]:

$$I_{on} \propto T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^{*}}E_g^{\frac{3}{2}}}{3q\hbar(E_g+\Delta\Phi)}\right) \quad (1)$$

where E_g is the semiconductor bandgap, m^{*} the effective mass, λ a screening length and $\Delta\Phi$ is the energetic difference between the conduction band in the source and the valence band in the channel for the P-TFET. Differents heterostructure have been proposed based on III/V or Si/Ge nanowires obtained by top-down [6–8], and bottom-up approaches [9–12] in order to reduce the SS and increase the Ion current. Moreover, group IV semiconductor is a preferred material for making TFET because they are easily integrable on a Si platform.

In this context, we present the fabrication and the electrical characterization of Ω-gate TFET devices based on horizontal p-Si/i-Si/$n^{+}Si_{0.7}Ge_{0.3}$ heterostructure and Si and $Si_{0.7}Ge_{0.3}$ homostructure nanowires grown by Chemical Vapor Deposition (CVD) using vapor–liquid–solid (VLS) mechanism. We demonstrate that the p-Si/i-Si/$n^{+}Si_{0.7}Ge_{0.3}$ heterostructure TFET devices present a very good electrical performance as compared to Si and $Si_{0.7}Ge_{0.3}$ homostructure devices. The best devices present an Ion current of about 245 nA at V_{DS} = −0.5 V and V_{GS} = −3 V with an SS around 135 mV/dec. Finally, we show that our electrical results are in good agreement with 3D numerical simulation using Kane's BBT model.

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2. Nanowires growth and fabrication of TFET devices

The axial p-Si/i-Si/n$^+$Si$_{0.7}$Ge$_{0.3}$ HT NW and p-i-n$^+$Si and Si$_{0.7}$Ge$_{0.3}$ homostructures NW were grown by low pressure chemical-vapor-deposition (LPCVD) using VLS mechanism with an in situ doping profile. The Au colloids (50 nm or 100 nm) drop-casted on Si (1 1 1) substrates were used as catalysts for size-calibrated NW's growth. For the Si NW, the growth was performed at 600 °C under a total pressure of 3 Torr using 40 sccm of Silane (SiH_4) and 100 sccm of HCl as reactive gases. For Si$_{0.7}$Ge$_{0.3}$ NW and axial heterostructure p-Si/i-Si/n$^+$Si$_{0.7}$Ge$_{0.3}$ NW, prior to the growth, the substrates were annealed at 650 °C and cooled down to the deposition temperature of 450 °C. These NWs grown under a total pressure of 4.5 Torr using 90 sccm of SiH_4 and 45 sccm of Germane (GeH_4) gas precursor and 40 sccm of HCl [13,14]. The doping modulation of NW is obtained by introducing the dopant precursors, B_2H_6 and PH_3 to p-type and n-type doping respectively, in addition to the other gas precursors. To carry out the axial heterostructure p-Si/i-Si/n$^+$Si$_{0.7}$Ge$_{0.3}$ NW, the growth started with Si p-type and intrinsic segment, followed by a 2 min growth interruption and after the Si$_{0.7}$Ge$_{0.3}$ n-type doped segment is grown. This growth strategy is the way to obtain a sharp interface between Si and Si$_{0.7}$Ge$_{0.3}$ part using Au-catalyzed VLS method as previously published in [15]. For all nanowires, the growth time is calculated to obtain a total NW length of about 7 μm including the p- and n-type segments of about 3 μm length and the intrinsic region of around 1 μm between both doped parts, as shown in Fig. 1. The main growth parameters are presented in Table 1. The doping level of each part of Si NW have been evaluated by a four point technique, in comparison with the silicon bulk resistivity. The p-type doping level is estimated to $5 \cdot 10^{18}$ cm^{-3} and the n-type doping level at 10^{19} cm^{-3}. The doping level of Si$_{0.7}$Ge$_{0.3}$ and Si parts grown at 450 °C are expected to be around 10^{19} cm^{-3} and $5 \cdot 10^{18}$ cm^{-3} respectively, with respect to the growth conditions listed in Table 1.

In order to fabricate TFET devices, gold catalyst was removed from the wires using successive dipping in HF, KI:I_2, HF bath. Then nanowires were suspended ultrasonically in an isopropanol solution and transferred to a Si wafer covered with a 100 nm thick silicon nitride. Optical lithography was used to define drain and source contacts. After development, contacts were cleaned in buffered oxide etchant (BOE) solution to remove native oxide on the NW, then it was metalized (Ni 80 nm/Al 120 nm) using e-beam evaporator. A lift-off step was performed to remove resist and an O_2 plasma step was used to clean the wires from all resist wastes which could perturb electrical transport. Subsequently, Alumina (Al_2O_3) was deposited by Atomic Layer Deposition (ALD) as gate oxide and then the top gate contact was defined using photo-lithography followed by metal deposition (the metal gate is Aluminium) and lift-off.

Table 1
Growth parameters of different nanowires.

	Full SiNW	Full SiGe	HT Si/Si/SiGe
T °C growth	600 °C	450 °C	450 °C
PH_3 ratio	$1 \cdot 10^{-3}$	$1.7 \cdot 10^{-3}$	$2.1 \cdot 10^{-3}$
B_2H_6 ratio	$1 \cdot 10^{-3}$	$5.3 \cdot 10^{-4}$	$1.7 \cdot 10^{-3}$
SiH_4 flux	40	90	90
GeH_4 flux	0	45	45

3. Experimental results and discussion

3.1. TFET characterization

Current–voltage (I–V) measurements were performed at room temperature and in dark conditions for Si, Si$_{0.7}$Ge$_{0.3}$ and Si/Si/Si$_{0.7}$Ge$_{0.3}$ nanowire TFET devices, using the Semiconductor Parameter Analyzer (HP4155). For all the I–V curves, the source contact (n^{++}-part) is grounded and a voltage was applied to the drain contact (p$^+$-part), such that a negative drain voltage V_{DS} corresponds to a reversed-biased p-i-n junction. All the currents are normalized by the NW circumference.

Silicon NW TFET has been fabricated as a reference device, as silicon material being well-known and extensively studied. This device has an equivalent oxide thickness (EOT) of 5.5 nm and the nanowire diameter of about 100 nm. First, we annealed the drain and source (D/S) contacts before the ALD oxide deposition, at 400 °C over H_2N_2 during 1 min in order to improve the drain/source contact resistance. The silicided parts have a length of about 100 nm for each contact, which doesn't reduce the channel length because of the D/S metallic contacts are separated by 4 μm and the channel length is of 1 μm. The transfer characteristics at $V_{DS} = -0.5$ V and $V_{DS} = -1$ V are shown in Fig. 2. For both drain voltages, the transfer characteristics are identical in the same gate voltage range. Only Ioff current at $V_{GS} = 0$ V weakly depends on the drain voltage, due to the SRH (Shockley–Read–Hall) recombination component, but it remains lower than 0.1 nA for

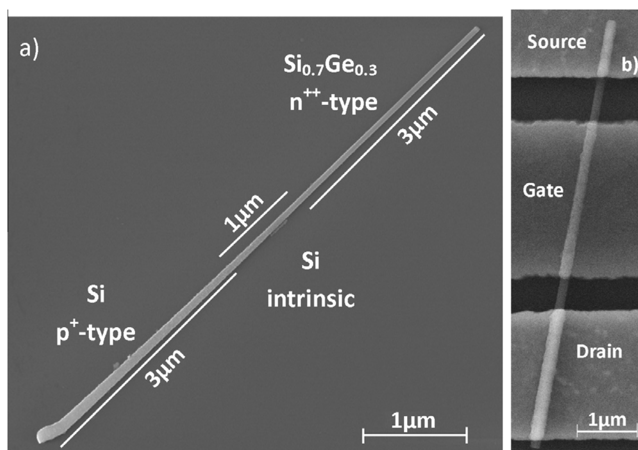

Fig. 1. (a) Scanning Electron Microscopy (SEM) picture of a p$^+$-Si/Si/n$^+$Si$_{0.7}$Ge$_{0.3}$ nanowire junction with a length of 7 μm and a diameter of 90 nm. (b) SEM picture of the Tunnel FET device on Ω-gate configuration.

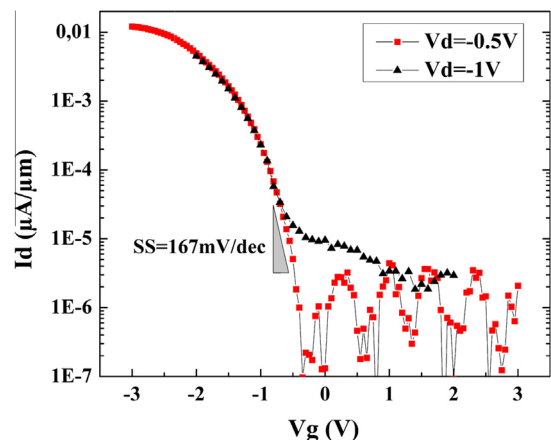

Fig. 2. Room temperature transfer characteristics in the semi-log scale of Silicon NW TFET at $V_{DS} = -0.5$ V (in square red) and at $V_{DS} = -1$ V (in black square). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

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