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Role of the gate in ballistic nanowire SOI MOSFETs

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ABSTRACT

In this paper we report the results of Monte-Carlo simulations performed on double-gate ballistic MOSFETs with a geometry such that the gates overlap only a fraction of the channel. We present a qualitative analysis of the simulation results highlighting the similarities and differences between ballistic devices of 10 nm and 100 nm channel length, in an attempt to understand the electrostatics in a ballistic channel, especially the influence of the gate, source and drain terminals on the channel.

1. Introduction

With device dimensions shrinking to sub-30 nm lengths, ballistic transport is increasingly gaining prominence. Ballistic transport in semiconductor devices occurs when the charge carriers emitted from one end (source) are collected at the other end (drain), without being scattered in the channel [1]. This is indeed similar to electron transport in vacuum tubes. In fact, ballistic n^+-n-n^+ semiconductors have even been shown to demonstrate the same *I–V* characteristics as the Langmuir–Child law [2] for vacuum tubes.

In addition to the scatter-free transport in their respective channels, according to the well-accepted virtual-source model of ballistic transport in MOSFETs, even the current control mechanisms in the vacuum tubes and ballistic MOSFETs is identical. Similar to the description of transport in vacuum tubes [3,4], the virtual-source model considers the top of the potential barrier that appears in the channel as an effective source of charge carriers (electrons) [5]. This virtual-source appears near the source end of the MOSFET and its height modulates the drain current. According to the model, in a scatter-free channel, the carriers injected from the source with energies higher than the virtual-source barrier pass through to the drain; the rest are reflected back. The carriers collected by the drain constitute the drain-current. While the source and drain voltages control the number of carriers injected into the channel,[1] the gate voltage controls how many of them pass through the channel by controlling the barrier height.

Even though the model very reasonably explains the transport and the current control mechanism, it does not provide a clear explanation of the role that the gate plays throughout the channel. From the above description it appears that the gate plays its role only locally at the virtual-source, like the grid in a vacuum tube. However, unlike the grid, the gate physically covers the entire channel of the MOSFET, and should affect the electrostatic potential at every point in the channel. In fact, the electrostatic control exerted by the gate at each point of the channel is imperative in a conventional diffusive MOSFET, where the transport is affected by the local quasi-Fermi potential. On the other hand, it can be argued that since transport in a ballistic device is non-local and the carrier populations are governed by the source and drain Fermi potentials [6] and not the local quasi-Fermi level in the channel, the gate need not play the same role as in the diffusive device. The carriers which manage to surpass the barrier at the virtual-source would continue their flight unimpeded (i.e., ballistically), exclusively under the influence of the drain-source electric field, and therefore, the influence of the gate should be limited only around the virtual-source. Consequently, we can wonder whether, in a ballistic MOSFET, a gate electrode that physically covers the channel only partially near the source would be sufficient to modulate the conduction in the device.

It is evident then that the role of the gate in ballistic MOSFETs is not clearly understood. In this paper we propose a MOSFET geometry such that the metal gate overlaps the channel partially. By exploring the possibility and consequences of using a partial gate

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[1] The carriers injected from the drain are suppressed at a drain-source voltage much higher than the thermal voltage.

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that does not affect the electrostatics along the entire channel, we aim to understand whether the gate in a ballistic MOSFET behaves like the grid in a vacuum tube, or like the gate of a conventional diffusive MOSFET.

We report results of Monte-Carlo simulations performed on idealized double-gate SOI MOSFETs with their gates overlapping various fractional lengths of the channel. The device geometry and simulation methods are described in the next section followed by a qualitative analysis of the simulation results in the subsequent sections.

2. Device templates and Monte-Carlo simulation

We ran Monte-Carlo simulations on idealized partially gated double-gate MOSFET whose geometry is shown in Fig. 1. This is a DG-MOSFET with a 5 nm thick Si body and 1 nm thick SiO_2 gate oxide. A metal gate with work-function 4.61 eV is used. The source and drain extensions are each 10 nm long and are n-type doped to 1.2×10^{20} cm^{-3}. The channel is considered undoped with a residual doping of 1.2×10^{15} cm^{-3}. Two different channel lengths (L_c =10 nm, 100 nm, and six different gate lengths (L_G/L_c = 0.1, 0.3, 0.5, 0.8, 0.9 and 1) were simulated.

Multi-Subband Ensemble Monte-Carlo (MSB-EMC) simulations were used to study the electrostatics and transport. The devices were made artificially ballistic by turning off all the scattering mechanisms in the channel region. The electrons are completely thermalized in the source and drain regions, i.e., they scatter in these regions, while they travel ballistically through the channel. In the semiclassical picture, depending on the respective bias voltages, the electrons can be visualized as being injected from the source and drain terminals. Under the influence of the applied electric field these injected electrons drift scatter-free but can be reflected at any potential barriers that they encounter. The reflected electrons are collected by the injecting terminal whereas the rest of the electrons are collected at the opposite terminal. Several quantities of interest like the electrostatic potential, electron density, average electron velocity etc. can be obtained as a result of these simulations.

The code used in this work is based on the space-mode approach of quantum transport [7], which provides one of the most detailed descriptions of carrier transport including in a natural way the ballistic behavior of ultra-short devices. This approach treats the transport as semiclassical and solves 1D Schrödinger equation for different slabs in the confinement direction. The electrostatics of the system is obtained from the coupled solution of 2D Poisson and 1D Schrödinger system. In this way, the evolution of the eigenenergies and wavefunctions for the i-th valley and the v-th subband is obtained along the transport direction. To evaluate the transport properties, the Boltzmann Transport equation (BTE) is solved by the Ensemble Monte Carlo method (EMC) considering a non-parabolic conduction band approximation in both confinement and transport directions [8]. This MSB-EMC simulator has been successfully applied for the study of different nanodevices including bulk [9], DGSOI [10] and FDSOI [11].

3. Discussion of the simulation results

In the following discussion we refer to the channel length L_c as the length of the semiconductor between the source and drain junctions while the gate length L_G is the length of the channel covered by the metal gate and is not necessarily equal to L_c. The x coordinate refers to the direction along the channel from the source to drain; the y coordinate refers to the direction between the gates.

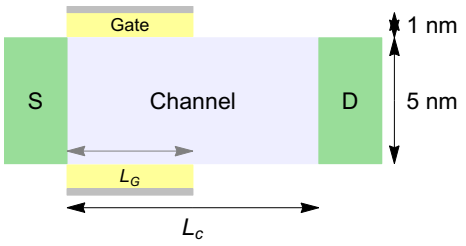

Fig. 1. Geometry of the partially gated DG-MOSFET used for the Monte-Carlo simulations. The channel length L_c is the length of the semiconductor between the source and drain junctions. The gate length L_G is the length of the channel covered by the metal gate. This structure was simulated for L_G/L_c = 0.1, 0.3, 0.5, 0.8, 0.9 and 1.

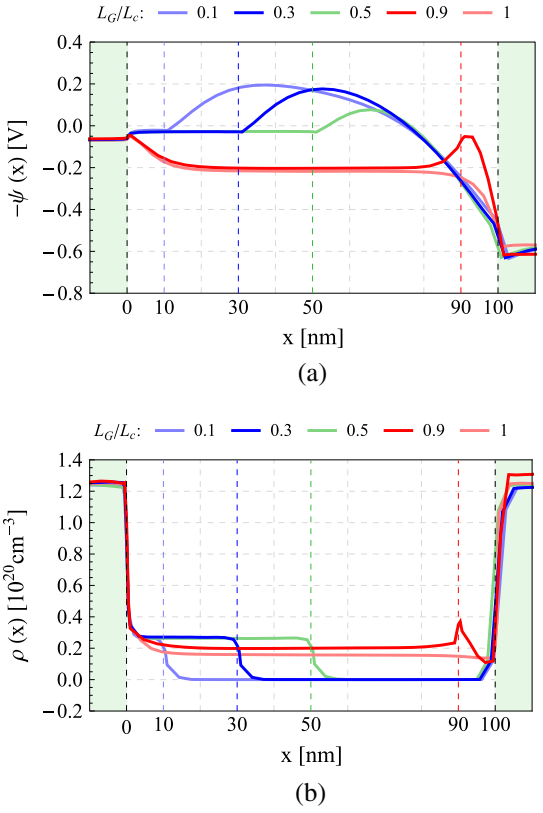

Fig. 2. Monte-Carlo simulation results for the 100 nm partially gated devices. (a) The potential profile. (b) The carrier density profile. L_c = 100 nm, V_D = 0.5 V, V_G = 1.0 V, ϕ_{ms} = 0.45 V. L_G/L_c = 0.1, 0.3, 0.5, 0.9 and 1.

Figs. 2 and 3 show the potential and charge profiles in the 100 nm and 10 nm channels respectively, for different gate lengths. The potential and charge profiles in the two devices with different channel lengths seem to be markedly different from each other. Even for a given channel length, L_c, devices with different gate length fraction, L_G/L_c, show different profiles; the differences among the 100 nm devices being more pronounced than between the 10 nm ones.

To understand the observed behavior let us consider the gated and the non-gated parts of the channel separately. Because of the presence of the gate, the potential in the gated part of the channel is governed by the 2-D Poisson's equation

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{q\rho(x,y)}{\varepsilon}, \quad (1)$$