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Analysis of heat dissipation of epitaxial graphene devices on SiC

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ABSTRACT

A three-dimensional thermal simulation for analysis of heat dissipation of graphene resistors on silicon carbide substrates is presented. We investigate the effect of parameters such as graphene–substrate interface thermal resistance, device size and source-to-drain contact spacing, to quantify lateral as well as vertical heat spreading. Pulsed *I–V* measurements were performed at different temperatures and pulse widths to extract device thermal resistance for comparison with simulation results. Due to small heat capacitance of the device, self-heating occurs even at the shortest pulse time of 200 ns. The effective thermal resistance of epitaxial graphene resistors on SiC was estimated as 8×10^{-5} K cm^2 W^{-1}, by comparison between measurement and simulation results.

1. Introduction

Graphene has been the topic of extensive research because of its superb electrical [1], mechanical [2], optical [3] and thermal [4,5] characteristics. In the r.f. and microwave area, extremely high electron and hole mobility [6,7] have made graphene an attractive candidate for the channel material of high speed devices. Various demonstrations of graphene RF transistors have proven graphene's potential for high frequency applications, based on outstanding carrier mobility, high saturation velocity and high carrier density [8,9]. However, in order to enhance the performance of many high speed devices, intense electric fields along with high current densities are needed in the channel, and consequently Joule heating occurs [10]. Although graphene has extremely good thermal conductivity [4], the overall heat dissipation of graphene devices is controlled by the thermal resistance of the system, which depends on the device structure, interface resistance, substrate material, etc. Understanding the heat spreading of graphene devices is important because self-heating effects can limit the effective carrier mobility of the graphene [11,12], maximum current carrying capability [13], and overall device reliability [14].

In this study, we conducted a three dimensional (3-D) thermal simulation to investigate the heat dissipation characteristics of representative device structures for r.f. applications. In order to compare our simulations with experimental results, pulsed current vs. voltage characteristics of graphene resistors were also measured under various temperatures and bias conditions.

2. Simulation methods and results

A physically-based device simulator (Sentaurus TCAD of Synopsys) was used for the 3-D simulation. We typically assumed a uniform heat source over the graphene resistor's 'channel' area. The baseline structure is a non-gated epitaxial graphene device [8] which has "source-drain" spacing L_{SD} of 500 nm, graphene channel width of 6 μm. A 300 K heat sink is located at the bottom of the SiC substrate, which is reduced to 50 μm in the simulation for efficient calculation. The insensitivity to SiC thickness is validated by comparing simulation for thicknesses up to 150 μm, which show less than 1% difference of T_{Max} from that of the 50 μm case used. A large volume outside of the device region was included to allow for 3D heat spreading. A quarter of the device was simulated for to decrease simulation time, thanks to the reflective boundary conditions. Fig. 1 shows a representative 3-D simulation structure (a quarter of the device) with zoom-in image of channel area with mesh grid (inset).

Reported parameters were used for thermal conductivity κ_{th} of graphene (50 W cm^{-1} K^{-1} [4]), SiC (4.9 Wcm^{-1}K^{-1} [15]), as well as for interface thermal resistance at the graphene–substrate interface (8.8×10^{-9} K m^2 W^{-1} [16]), and at the graphene–metal interface (1.92×10^{-9} K m^2 W^{-1} [17]). The interface thermal resistance is also known as Kapitza resistance, which is thought to originate from differences of electronic and vibrational properties

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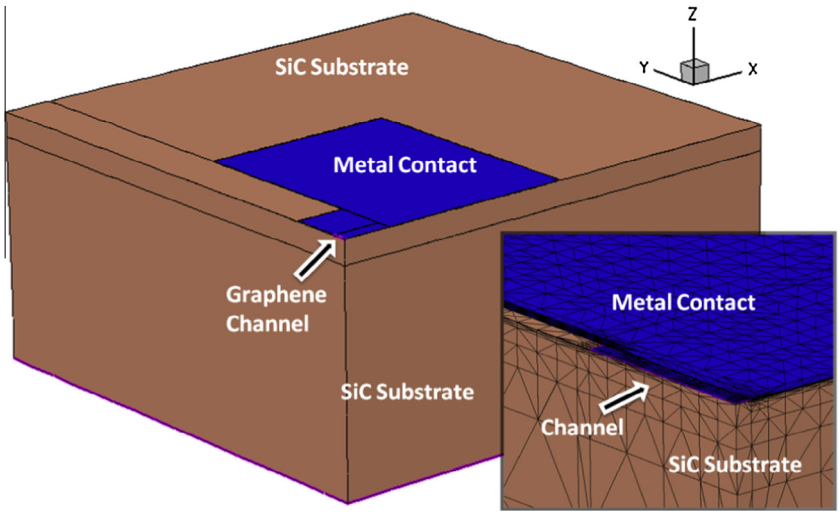

Fig. 1. Simulated device structure; a quarter of graphene resistor on SiC substrate. (inset) Zoom-in image of the device with mesh grid.

of attached materials [18]. Heat transfer is hindered at the interface by the differences of phonon frequencies and vibrational characteristics between the two materials. The bulk thermal conductivity of 6H–SiC has been measured to be in the range 2.9–4.9 W cm^{-1} K^{-1} [15,19,20]; uncertainties in this value will affect the simulation by less than 10% of maximum temperature differences. For graphene, also, thermal conductivity values are also reported over a wide range according to various circumstances, such as graphene supported by SiO_2 and suspended graphene devices (50–5500 W m^{-1} K^{-1} [4,5,21,22]). It is also reported to have reduced thermal conductivity in the case of devices in ballistic regime [23]. In epitaxial graphene films, it is likely that the mean free path of phonon will decrease due to the substrate scattering [24,25], therefore it may not reach the ballistic limit until the device is scaled down to less than 100 nm. In this paper, we assumed the graphene thermal conductivity value to be 50 W cm^{-1} K^{-1} with for graphene layer of 0.35 nm thickness.

Fig. 2(a) displays the lattice temperature distribution for uniform DC power dissipation over the channel area. A zoom-in image (b) and a cut-area picture (c) indicate better cooling near the metal contact and the edge of the graphene. Because of the lateral heat spreading into metal contacts and edges of the device, the maximum "junction" temperature (T_{Max}) can be found at the middle of the device channel, when the heating is occurring uniformly over the channel area.

Overall thermal resistance of the device is highly impacted by the bulk thermal conductivity of the substrate [16], because the heat spreads through the substrate to reach the bottom heat sink. In our simulation, the heat sink is only located at the bottom of substrate, which is also valid in most real devices. Cooling by air convection from the top surface is not considered in this study. When the substrate material is fixed, the graphene–substrate interface thermal resistance (R_{int}) becomes an important factor. The relation of input power density (P_{in}) to T_{Max} is shown in Fig. 3(a) for several R_{int} values. T_{Max} is 380 K (80 K temperature rise) for P_{in} of 1×10^6 W/cm^2, when $R_{int} = 8.8 \times 10^{-9}$ K m^2 W^{-1} [16] (corresponding to the assumption that graphene layer and SiC substrate interface thermal resistance has approximately the same value as for the graphene–SiO_2 interface). Even if R_{int} is smaller than expected thermal resistance of hydrogen passivated interface, it shows significant effect on temperature rise compared with assuming no interface resistance. R_{int} of 8.8×10^{-9} K m^2 W^{-1} is an example of non-zero, however, order of magnitude smaller interface resistance than SiO_2 case. In the following, $R_{int} = 8.8 \times 10^{-9}$ K m^2 W^{-1} is assumed. The impact of the thermal conductivity of the graphene film is shown in Fig. 3(b), where the temperature rise is shown for the case of $R_{int} = 8.8 \times 10^{-9}$ K m^2 W^{-1} at 10 mW/μm^2 input power. The graphene thermal conductivity is observed to have only a minor effect on overall temperature rise.

The effect of lateral heat spreading and 3-D heat spreading can be seen in Fig. 4. Fig. 4(a) shows the 2-D structure of simulated devices with various channel lengths and uniform power input over the whole channel (for example, when the sheet resistance of graphene channel is uniform and same amount of current is applied across the channel length). T_{Max} vs. uniform power input density of P_{in} over the channel is described in Fig. 4(b). As channel length increases while the power density is fixed, heat spreading from the middle of the channel becomes more difficult because lateral spreading is suppressed and vertical heat spreading is also limited to 1D, rather than 3D, heat spreading. Since the power density is uniform, the total amount of power is also larger for long channel cases.

Most of the heat arriving at the metal contact conducts laterally through thick metal films, eventually spreads into the substrate. In order to determine the paths of heat spreading, one can integrate the heat flux of each interface. According to the simulation, the majority of the heat spreads vertically into the substrate while only a small amount of heat is relieved laterally by source and drain contacts, even for short channel lengths. The lateral heat diffusion component along the graphene layer is ~14% out of total power input for L_{SD} = 100 nm and only ~1% for L_{SD} = 500 nm. This ratio will be decided by contact distance, thermal conductivity of bulk substrate and interface, for instance, lateral heat spreading will be more helpful when the substrate's thermal conductivity is low, such as SiO_2.

A localized heating area simulation can show the impact of contact spacing on lateral heat spreading. The simulation schematic is described in Fig. 5(a and b), where we applied 50 nm length and 6 μm width of limited local heat source at the middle of the channel length of 100 nm and 500 nm, respectively. This allows the same total power input for devices with different contact spacing. Even though the absolute temperature rise in Fig. 5(c and d) is smaller than in Fig. 4(b) due to limited heating area and 3-D heat spreading, short channel devices have more benefit (~15% lower T_{Max}) from the lateral heat spreading into metal contacts. The limited relief to the hotspot in the middle of the channel is reduced with longer L_{SD}. Lattice temperature profile is also described in Fig. 5(a and b), which can be fitted by $T(x) = T_0 + T_{Max} \cdot e^{-|x|/L_c}$,