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A new non-volatile memory architecture embedding microbatteries to improve data retention criterion

J. Postel-Pellerin *, P. Chiquet, F. Lalande

Aix-Marseille University, IM2NP-CNRS, UMR 7334, IMT Technopole de Chateau-Gombert, 13451 Marseille, France

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ABSTRACT

In this paper, we propose an original Flash-type structure, integrating microbatteries in the circuitry to localize the stored charge over a thick oxide during the retention phase and thus improving this key reliability criterion. We first describe the proposed architecture using two lateral gates and different programming and erasing schemes. Then we develop a full TCAD simulation of our structure showing the feasibility of this cell with a viable 3.2 V programming window before process optimization. Moreover, through recent advances in micro–nanobatteries, we demonstrate that we are able to integrate them in the circuitry to maintain 10 Gbytes worth of data for more than ten years.

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1. Introduction

As Non-Volatile Memory (NVM) technology gains maturity, its use becomes more widespread and new application fields emerge. Often, these new applications imply new product requirements, as in the automotive case where reliable operation at 125 °C is mandatory and there is an increase in the number of specific operations at temperatures up to 190 °C. The study of the electrical behavior of memory cells with temperature, and particularly their reliability, has become a major issue. The cell retention, which is the capacity of a memory cell to conserve information when power supply is off, is a key criterion for reliable cells. When considering an NVM cell with a floating gate (Fig. 1), such as EEPROM or Flash cells [1], the threshold voltage V_T is shifted according to Eq. (1):

$$V_T = V_{T0} - \frac{Q_{FG}}{C_{pp}} \quad (1)$$

where V_{T0} is the natural threshold voltage of the cell, Q_{FG} the charge amount in the floating gate and C_{pp} the interpoly capacitor between the control gate and the floating gate, both in PolySilicon.

Q_{FG} quantity is injected into the floating gate by applying an adequate set of biases to the transistor terminals, depending on technology (Flash or EEPROM) [2–5]. During these programming phases, currents pass through tunnel oxide located between the floating gate and the drain area. This oxide has an antagonistic role: avoiding electric charge leakage while being transparent enough during programming steps. Thus the quality of dielectrics has a major role in the reliability of the whole device. As previously detailed in Eq. (1), charge loss phenomenon is directly linked to electrons leaking from the floating gate, decreasing the total number of stored electrons and so inducing a progressive data loss [6–8]. In order to improve this reliability criterion, two major ways can be followed. The first one consists in understanding the leakage paths and mechanisms to decrease the oxide degradation and thus increase the cell lifetime. Many previous studies have already dealt with this topic but some of them seem to show a leakage through SiO_2 tunnel oxide [9,10] while others seem to show other leakage paths through the tri-layer stack oxide Oxide/Nitride/Oxide (ONO) [11,12]. Another approach consists in creating and developing new non-volatile memory designs, with a higher robustness against charge leakage, such as for example nanocrystal non-volatile memories [13] or SONOS memories [14]. In this paper we will describe a new cell design using a continuous floating gate architecture (Flash-type) and allowing to maintain the stored charge for longer durations, thanks to integrated microbatteries. The use of a continuous floating gate has the main advantage that we can re-use well-known Flash process recipes and models, without having to develop new heavy process steps (nanocrystals growth for instance).

2. New proposed Flash-type architecture embedding microbatteries

The proposed cell is based on a classical Flash design for which the first N+ doped PolySilicon layer is divided in three parts, separated by a thin oxide, as shown in Fig. 2. The central floating

* Corresponding author.
E-mail address: jeremy.postel-pellerin@im2np.fr (J. Postel-Pellerin).

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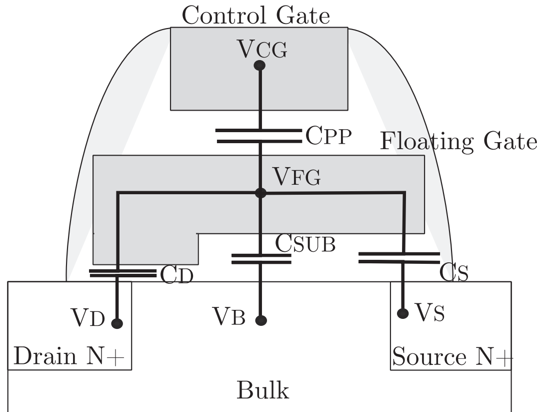

Fig. 1. Schematic of capacitances in a floating gate NVM.

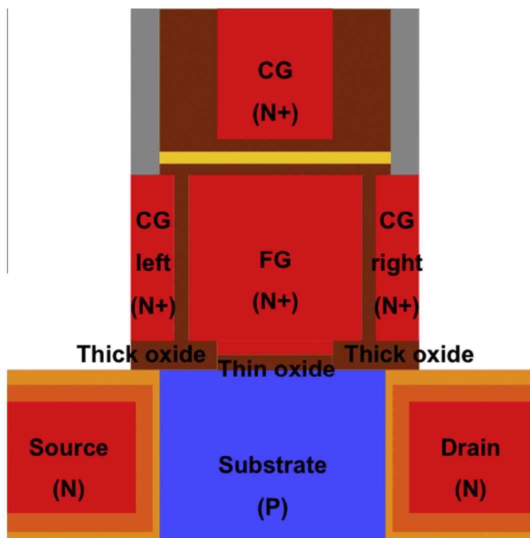

Fig. 2. Schematic view of the proposed structure.

gate (FG) will be used to store the charges injected during programming and erasing operations while the two lateral control gates (CG) will be used mainly during the retention phase. We can also remark that the tunnel oxide between the FG and the channel has not a constant thickness. Indeed it is thinner in the middle (around 7–8 nm) than at the sides (around 15 nm).

The thinner part will be used to inject charges in the floating gate while the thicker part will be used to retain charges during retention thanks to the addition of microbatteries in the circuitry which will allow to keep a positive bias on the two lateral gates, attracting electrons at the sides of the central FG over the thick oxide and thus reducing the charge leakage through tunnel oxide. Moreover, this positive bias will decrease the floating gate potential according to Eq. (2), also reducing the charge leakage as demonstrated in [15]. We will detail the integration of these microbatteries in Section 3.

$$V_{FG} = \alpha.V_{CG} + \frac{Q_{FG}}{C_{TOT}} \quad (2)$$

where, using notations from Fig. 1, $C_{TOT} = C_D + C_{SUB} + C_S + C_{pp}$ and $\alpha = \frac{C_{pp}}{C_{TOT}}$ the coupling ratio.

2.1. Programming and erasing the cell

Programming and erasing operations use the Fowler–Nordheim mechanism [16], which can even be enhanced thanks to the two lateral CG. In Fig. 3(a), we can see that we apply a high positive bias V_{prog} on the top Control Gate to inject electrons into the floating gate by using Fowler–Nordheim tunneling current. Nevertheless the injection zone is too small to have an efficient programming phase so we also bias the two lateral Control Gates at V_{prog}. Due to the shape of the Control Gates, surrounding the Floating Gate, the coupling ratio of the cell is highly increased (around 0.75) compared to the typical values obtained for Flash cells (around 0.6) and we should obtain a sufficient programming threshold voltage even decreasing V_{prog}. We expect to decrease the programming voltage down to 14 V, instead of 17 V in a typical NAND Flash cell using FN mechanism [17]. To erase the cell, we can first simply use the reverse phenomenon by biasing the Source/Substrate/Drain contacts at $V_{prog} = 14$ V, grounding the three Control Gates, as presented in Fig. 3(b). As previously discussed for the programming phase, the efficiency is not very good but it can also be improved by biasing the lateral Control Gates at V_{prog}. Indeed, as mentioned earlier in this section, a thin oxide separates the FG and the two lateral CGs, enabling FN tunneling. Fig. 3(c) shows this enhanced erasing phase. Moreover, concerning reliability issues (endurance and retention), if we inject electrons into the floating gate through tunnel oxide and remove them through lateral oxides partially, it could improve the reliability of our cell because we do not always damage the same oxide and charges should be thus better injected and trapped in the floating gate. This cell structure could also be optimized to be programmed through Channel Hot Electron mechanism [16] to be embedded in a NOR architecture but we will only focus on the full Fowler–Nordheim functioning.

2.2. TCAD simulation of the functioning on the proposed cell

This new proposed structure has been simulated in a classical TCAD simulation tool (Synopsis Sentaurus Structure Editor [18]). The thin SiO_2 oxide has a thickness of 8 nm while the thick SiO_2 oxide has a thickness of 15 nm. The N+ doped *PolySilicon* floating gate has a width of 60 nm in the upper part and 40 nm in the lower part (above the thin oxide) and is separated from the N+ doped *PolySilicon* lateral control gates by a 5 nm SiO_2 oxide. The control gate is above a tri-layer stack Oxide/Nitride/Oxide (5 nm/5 nm/5 nm) ans is 40 nm wide. It is separated from the aluminum via, connected to the lateral control gates, by a 20 nm thick oxide to reduce the parasitic capacitance between the control gate and the lateral control gates. The two Polysilicon layers are 100 nm high. The simulated structure is presented in Fig. 4, where the color scale corresponds to the doping concentration (red = N type, blue = P type).

The Synopsis Sentaurus Device electrical simulation tool is then applied to the previously simulated structure to perform the programming step (duration = 200 µs) and erasing step (duration = 1 ms) with biases from Fig. 3(a) and (c) respectively. The model used during the programming/erasing phases simulation is the Hydrodynamic model, commonly used in Flash memory simulations [19]. We performed a transient simulation to take into account the temporal evolution of the charge into the floating gate and the impact of the pulses' duration. Then we simulate the reading of the memory cell using the cell in the three different states (virgin: $Q_{FG} = 0$, programmed: Q_{FG} = final charge after the simulated programming step and erased: Q_{FG} = final charge after the simulated erasing step) by applying $V_{DS} = 2$ V and varying V_{CG} from 0 V to 8 V. The obtained Drain current versus Control Gate voltage characteristics of the virgin (no charge in the floating gate), programmed and erased cells are plotted in Fig. 5.

We can notice that when reading the threshold voltage of our memory cell at a current level around 1μA, we obtain a promising programming window (difference between the programmed and erased threshold voltages) of 3.2 V, which is a viable value for a

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