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Parametric amplifier based dynamic clocked comparator ☆

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ABSTRACT

The dynamic clocked comparator using a parametric amplifier is proposed and designed using a concept of the charge transfer amplification (CTA). A low gain (5 V/V) reverse discrete-time parametric amplifier (RDTPA) was used as a pre-amplifier stage of the proposed comparator. The level shifter scheme to nullify an input common-mode voltage (V_{CMI}) shows minimal deviation for varying process corners. The complete design including the latch and the RDTPA is designed and fabricated in an STMicroelectronics 32 nm CMOS technology with the supply voltage of 1 V and a sampling frequency of 50 MHz. The fabricated chip results show 7 mV of an input offset voltage, 120 μW of power consumption and 2.4 pJ of energy per comparison.

1. Introduction

A discrete-time parametric amplifier (DTPA) [1] can sample, hold and amplify an input signal using the MOS varactor properties. The DTPA consumes ultra low power with very low noise. A DTPA exhibits a common-mode voltage shift at the output terminal. To nullify this common-mode voltage shift [2], has proposed a complementary parametric amplifier (CDTPA). In a CDTPA, an nMOS-DTPA and a pMOS-DTPA act as loads to each other. In [2], a gain-boosted double complementary parametric amplifier (DCDTPA) has been proposed. The gain boosting in a DCDTPA is achieved through a reverse connected parametric amplifier (RDTPA).

In [3], a charge transfer amplifier has been designed as a pre-amplifier stage of the dynamic clocked comparator. An additional CTA stage at the input of a comparator reduces an input offset voltage by the factor of an amplifier-gain. The demonstration of a nullified common-mode output voltage shift for a DTPA based comparator has been implemented in [4,5]. However, the technique is sensitive to the varying process, voltage and temperature corners. In this paper, the common-mode voltage nullification scheme for a varying process, voltage and temperature is proposed and designed using the anti-parallel connected RDTPA. The concept has been demonstrated with the experimental chip results.

The paper is organized as follows. Section 2.1 explains the working principle of a DTPA. In Section 2.3, the working principles of anti-parallel connected parametric amplifiers is explained. In Section 3, the RDTPA based comparator is introduced and explained. The discussion on the proposed comparator on the basis of experimental results are the part of Section 4. The paper is summarized with a conclusion in Section 5.

2. Discrete-time parametric amplifier

2.1. Working principle of a DTPA

Fig. 1(a) shows a single ended DTPA. The DTPA operates over three phases viz. the track, the hold and the boost phase with the two non-overlapping clocks ϕ_1 and ϕ_2 (Fig. 1(b)). During the track phase, ϕ_1 and ϕ_2 are at high and low potential respectively. The source–drain (S–D) terminal of an nMOS transistor M_1 is connected at ground potential. An amplitude of the applied input signal is $V_{CMI} + v_{in}$, assuming the DC-bias voltage V_{CMI} is strong enough to keep M_1 in the strong inversion mode. With the small signal voltage v_{in}, the small-signal charge developed on the gate terminal of M_1 is $C_{si}v_{in}$. C_{si} is the total gate capacitance in strong inversion.

During the hold phase, both ϕ_1 and ϕ_2 are at low potential. The switches are turned off through ϕ_1 and by ϕ_2 and the S–D terminal of M_1 remains at the low potential. The tracked input remains held on the gate-terminal of M_1 in the hold phase.

During the boost phase, ϕ_1 is at low potential and ϕ_2 is at high potential. Because of low potential of ϕ_1, the input signal is no more connected to the circuit and now the load capacitance C_L is

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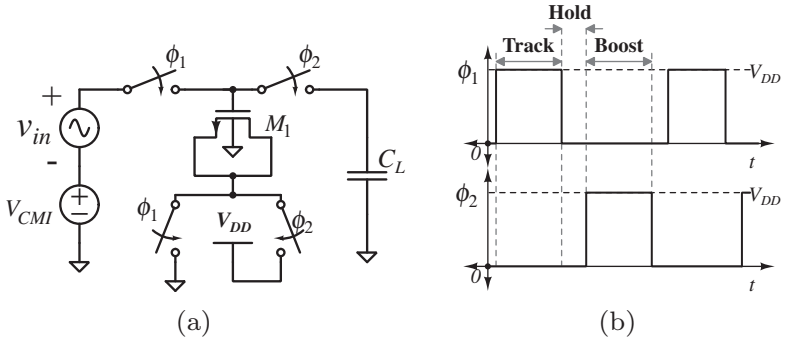

Fig. 1. (a) Schematic of a single-ended DTPA, (b) the timing diagram.

connected to the gate of M_1. The load capacitance C_L is assumed to be much smaller than C_{si}. During this phase of operation, the S–D terminal of M_1 is connected to the supply voltage V_{DD}. As per charge conservation law, the charge in the boost phase has to remain unchanged from the hold phase. Because of the large potential at S–D terminal of M_1, the mobile negative inversion charges of the oxide layer are attracted to the V_{DD} at the S–D terminal. The inversion layer of M_1 disappears due to the strong body effect resulting from pushing its source/drain of M_1 to V_{DD}, which reduces the gate capacitance from C_{si} to C_{wi}. C_{wi} is the total gate capacitance in weak inversion. Hence, the effective capacitance at the gate terminal of M_1 reduces. Therefore, the output voltage at the gate of M_1 increases. An amplification factor depends upon the ratio of the capacitance of the track/hold phase to the boost phase.

2.2. Q–V relationship

Fig. 2 [1] shows graphical representation of the Q–V characteristic of an nMOS DTPA and a pMOS DTPA. The Q–V relationship follows the dotted line in the track phase when V_{SB} is zero whereas the solid line represents the boost phase when $V_{SB} = V_{pull}$. V_{pull} is the applied voltage to pull out the inversion charges from the channel of a transistor during the boost phase of operation. The slope of a dotted line is C_{si} whereas the slope of a solid line is C_{wi}. The ratio of C_{si} to C_{wi} determines the gain of the parametric amplifier. The typical unloaded gain of a parametric amplifier varies between 5 and 10 V/V depending on the fabrication process. Fig. 2(a and b) exhibits an output voltage range of V_{DD} for both nMOS and pMOS DTPA. V_{CMI} and V_{CMO} are the average input voltage and the average output voltage respectively. The Q–V characteristics of an nMOS-DTPA (Fig. 2(a)) shows the positive average voltage shift whereas the pMOS based DTPA contributes the negative average voltage shift (Fig. 2(b)). This limits the utilization of the nMOS or the pMOS based DTPA in the applications of cascading of stages.

Fig. 2(c) shows the output of a single-ended nMOS DTPA as compared to its input. A gain of up to 5 may be observed in simulation for an STMicroelectronics 32 nm CMOS process. The boost phase of the DTPA can be identified with a large shift in the average voltage (V_{CMO}). The simulated DTPA has a 0.35 V average voltage shift during the boost phase. The large average voltage shift makes it difficult to connect two DTPAs in cascade, as this might saturate the output of the second DTPA to the power supply voltage.

2.3. Anti-parallel connected discrete-time parametric amplifier

Fig. 3(a and b) shows the schematic of a single ended complementary configured DTPA. To nullify the DC output voltage shift (V_{CMO}), a negative DC voltage shift pMOS-DTPA is connected as a load to the positive DC voltage shift nMOS-DTPA. For an exactly matched nMOS- and pMOS-DTPA capacitor, the characteristics shows $V_{CMI} = V_{CMO}$ when $V_{CMI} = V_{DD}/2$. During the track phase, the input voltage (V_{CMI}) of the CDTPA determines the total charge on the nMOS and pMOS gates. During the boost phase, the total charge remains the same and V_{CMO} is determined by the boost-phase characteristics (assuming absence of any other load). For an identical capacitance of the nMOS-DTPA and the pMOS-DTPA, the V_{CMO} is $V_{DD}/2$ when the V_{CMI} is fixed at $V_{DD}/2$. Moreover, the use of anti-parallel connected parametric amplifiers helps in getting amplification for a differential input signal. The slope of the Q_G–V_G characteristics during the boost phase to the slope of the Q_G–V_G characteristics during the track phase determines the gain

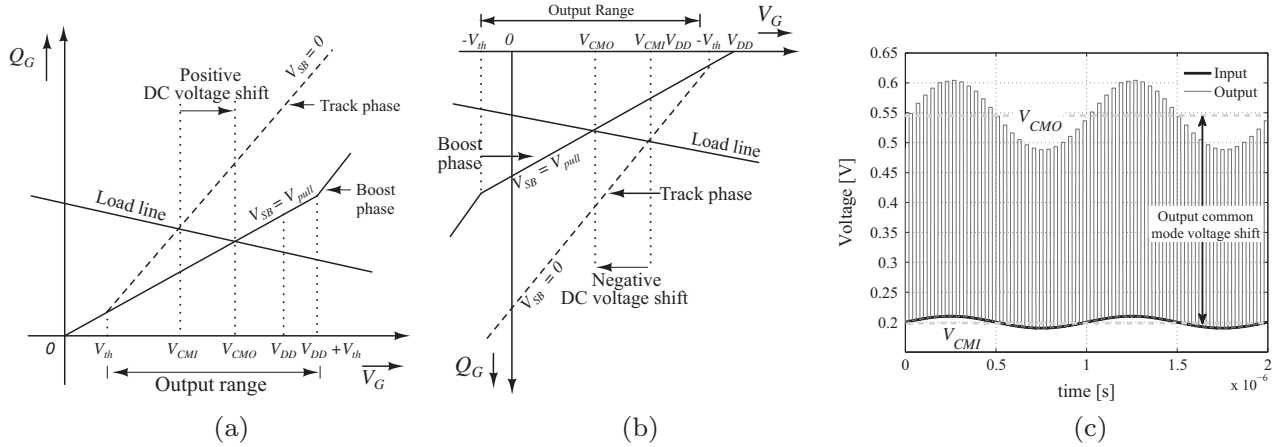

Fig. 2. The Q–V characteristics [1] of (a) the nMOS-DTPA (b) the pMOS-DTPA and (c) output of a single-ended DTPA for v_{in} of 25 mV amplitude and V_{CMI} of 200 mV.