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Negative Bias Temperature Instabilities induced in devices with millisecond anneal for ultra-shallow junctions

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ABSTRACT

In this paper the NBTI degradation has been studied in pMOS transistors with ultra-thin high-*k* dielectric subjected to a millisecond anneal for ultra-shallow junction implantation using different laser powers. An ultrafast characterization technique has been developed with the aim of acquiring the threshold voltage (V_{th}) shift in relaxation times as short as possible once the electrical stress is removed. It has been observed that increasing the millisecond anneal temperature reduce the NBTI degradation. These results have been explained in the context of the emission and capture probability maps of the defects.

1. Introduction

Ultra shallow junction formation in deeply scaled CMOS technologies requires the optimization and control of the implanted dopants. To achieve this objective millisecond anneal (MSA) has been shown to be a promising technique for the 32 nm node and below [1,2]. On the other hand, Negative Bias Temperature Instability (NBTI), which is characterized by a progressive shift of the transistor threshold voltage (V_{th}) when high gate voltage is applied, is one of the main aging mechanisms in CMOS devices [3,4]. NBTI is associated to charge in trapping defects when a high voltage is applied to the gate of the transistor and is especially relevant at high temperatures [5]. The charge in some defects can be rapidly detrapped, leading to a partial recovery (relaxation) of the damage created by the NBTI stress [6]. The fast NBTI relaxation makes difficult the characterization of this failure mechanism, being necessary the use of special techniques to correctly evaluate the real damage produced by the NBTI stress [7]. Moreover, NBTI is strongly dependent of the fabrication process [8]. In this regard, millisecond anneal (MSA) has been demonstrated to affect NBTI aging [9]. Here we will extend the NBTI relaxation studies, from very short to medium relaxation times, using a new ultra-fast (UF) technique to more accurately characterize the recovery of the NBTI degradation. Moreover, the results will be interpreted in the framework of the recent advances in the NBTI physics modelling.

2. Samples and the experimental set-up

The samples used in this work were pMOS transistors with $HfSiO/Al_2O_3$ dielectric (EOT ~ 14–15 Å [1]), TaCN as gate electrode and W/L = 10 μm/0.15 μm. The MSA considered applying laser pulses with low (LLP), medium (MLP) and high (HLP) laser powers. The temperatures achieved during the three types of annealing are estimated to be 1100 °C, 1200 °C and 1350 °C, respectively and the duration of each anneal was around 1 ms. To analyze the effect of MSA on NBTI, the transistors were electrically stressed with a constant voltage stress (CVS) sequence of 10 s, 100 s and 200 s applied to the gate to provoke the NBTI degradation. The stress voltages (V_{stress}) ranged from −1.8 V to −2.4 V. During the stress sequence the drain, source and bulk terminals were grounded. After each CVS time interval, the devices were relaxed for 150 s and the threshold voltage (V_{th}) was measured during the NBTI relaxation period using the ultra-fast (UF) set up developed in this work. All measurements were made at room temperature.

To acquire the NBTI relaxation, the UF measurement set-up depicted in Fig. 1 has been developed in order to register the device V_{th} in times as short as possible after the stress removal. The

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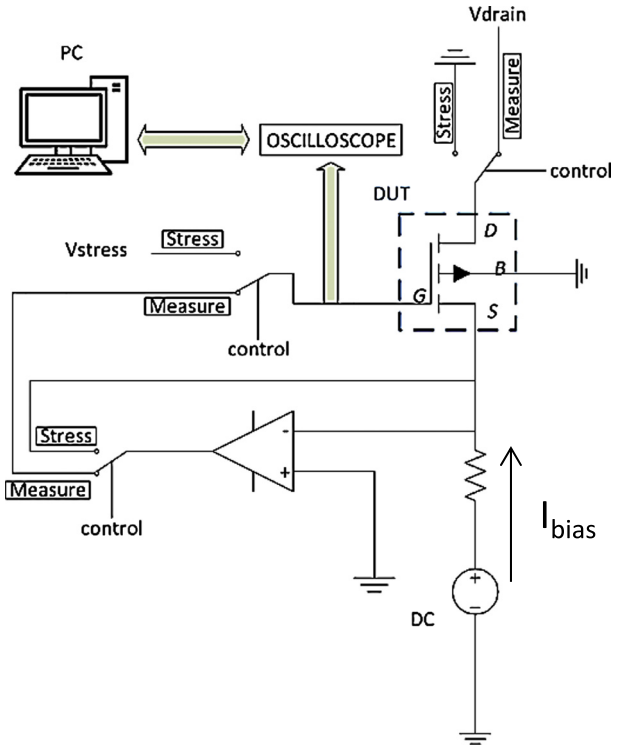

Fig. 1. Ultrafast setup developed to apply a stress voltage to the gate of the MOSFET under test and to measure the threshold voltage shift when the stress is removed. A feedback loop and the switches in the 'measure' mode force a constant voltage at the gate which is approximately equal to the threshold voltage, which is acquired by means of an oscilloscope probe.

shorter the first data acquisition time, the better the accuracy prediction of the NBTI degradation. The developed circuit has been designed with the aim of avoiding the open loop operation of the operational amplifier at any moment during the stress and relaxation process. This avoids voltage ripples that could be detrimental for the measurement. The circuit presented in Fig. 1, together with an instrumentation system control, is capable of applying an electrical stress (stress mode) on the gate terminal and subsequently measuring the V_{th} of the Device Under Test, DUT, (measure mode). By means of three switches the stress and measure sequences are controlled. When the switches are in the stress position, the stress voltage is applied to the gate of the DUT with the drain, source and bulk grounded, which provokes the device degradation. In this case the current through the channel is zero because I_{bias} flows through the operational loop. When the circuit is switched to the measure mode, a low drain voltage is applied to the drain, while bulk and source are grounded. In addition, a current through the channel is forced by means of I_{bias}. If the value of I_{bias} is properly chosen, the transistor operates at $V_{gate} \sim V_{th}$. The gate voltage in the 'measure' mode (i.e., the device V_{th}) will be acquired by means of an oscilloscope probe and transmitted to a computer by GPIB bus to analyze the signal. All the switches are controlled by means of an instrumentation system and the 'control' signal.

Fig. 2 shows an example of a typical oscilloscope capture of the gate voltage when the UF technique is used. The sample had a HLP annealing passivation and the stress voltage was −2.1 V. The switching from 'stress mode' to 'measure mode' is produced at time equal to zero. During the stress phase, the oscilloscope registers the stress voltage applied to the gate. When the circuit operation is switched to the measure mode, the gate voltage rapidly changes from the stress voltage to the threshold voltage (V_{th}) of the transistor. Using this set-up, measurements can be done for times as small as 20 μs, which allow obtaining information on the NBTI

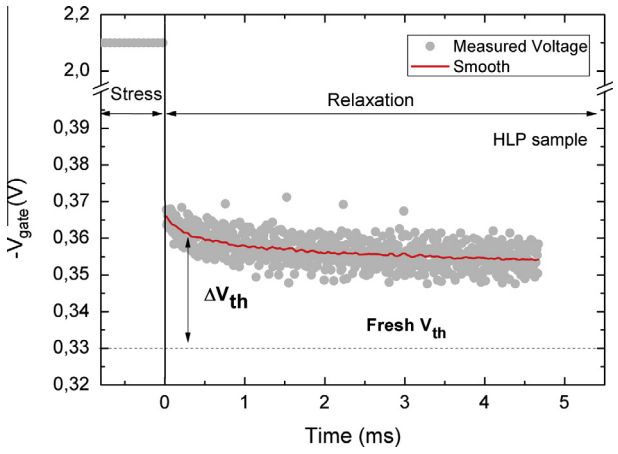

Fig. 2. Oscilloscope view obtained with the set-up in Fig. 1. During the stress phase, V_{stress} is measured, and once the circuit is switched to the measurement mode, the V_{th} of the transistor is recorded.

effects for very short relaxation times. The large quantity of data provided by one capture of the oscilloscope can be used to smooth the signal and get higher accuracy in the V_{th} trace. The total V_{th} shift (ΔV_{th}) induced by the NBTI degradation can be easily calculated as the difference between the measured voltage and the V_{th} values measured prior to the stress (fresh V_{th}). As can be observed in Fig. 2, immediately after the stress, a shift in V_{th} has been produced due to the NBTI degradation induced during the stress. The V_{th} recovery during the relaxation can be clearly observed. Then, the set-up in Fig. 1 is useful to characterize the NBTI degradation at very short times after the stress and it has been used for the study of the influence of the MSA on the NBTI.

3. Results

Fig. 3 shows the fresh (non-stressed) I_D–V_G characteristics in linear (left) and semilog (right) scale measured on a device subjected to LLP, MLP and HLP MSA. Clearly, a lower V_{th} is observed for MLP and HLP conditions which suggests a lower defect density when the anneal temperature increases. Fig. 4 shows the experimental NBTI relaxation traces (symbols) after stresses applied to the pMOS samples with different laser power MSA. The symbols until ~0.5 ms correspond to the first fast data block captured by the oscilloscope. After that, successive acquisitions were done up to 150 s of relaxation in order to measure the NBTI

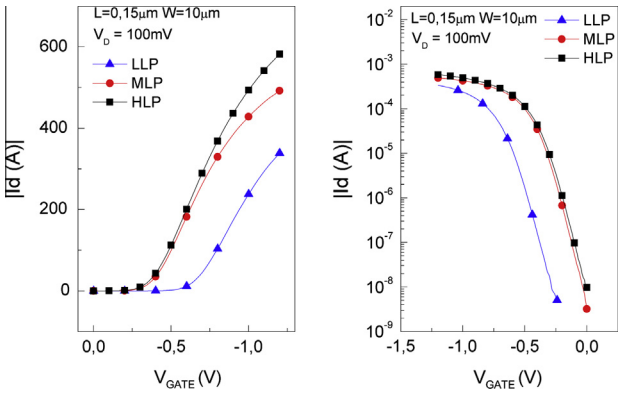

Fig. 3. pMOS fresh I_D–V_G curves measured in transistors with W/L = 10 μm/0.15 μm at room temperature, after the MSA. The data is plotted in linear (left) and semilog (right) scales.