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On the g_m/I_D-based approaches for threshold voltage extraction in advanced MOSFETs and their application to ultra-thin body SOI MOSFETs

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ABSTRACT

In this paper, we investigate the transconductance-to-current ratio (g_m/I_D) methods for the threshold voltage extraction using two popular threshold voltage criteria applicable to advanced bulk and SOI MOSFETs, namely: the condition of the maximum of the second derivative of the inversion charge and of the equality of the drift and diffusion drain current components. Using analytical modeling, we derive the first-order electrical parameters matching these two physical conditions and show that in the ideal MOSFET they do not coincide. The first corresponds to the point on the g_m/I_D versus gate voltage (V_g) curve where $d(g_m/I_D)/dV_G$ exhibits a minimum and where the ratio of g_m/I_D to its maximum value is equal to 2/3, whereas the second is met at the point where this ratio equals 1/2. The g_m/I_D methods for the V_{TH} extraction using the above two criteria and their correlation with other methods are discussed. Since our modeling is based on the unified charge control model, its predictions are expected to be valid for both bulk and SOI MOSFETs. Experimental and simulation results for advanced SOI MOSFETs are used to validate modeling derivations and clarify practical applicability and limitations of the g_m/I_D methods.

1. Introduction

The threshold voltage (V_{TH}) is a fundamental parameter of a MOSFET, which defines the transition between weak and strong inversion regimes (i.e., linear-to-exponential charge control). Therefore, the proper V_{TH} determination and its accurate extraction from the experimental characteristics are very important for CMOS device/circuit design and modeling, assessment of the variability of the fabrication processes and reliability issues. Presently there are a variety of V_{TH} extraction methods, which differ by the used extraction procedures and frequently yield different V_{TH} values for the same device [1–7]. The reason is their different sensitivity to the parasitic effects and different underlying V_{TH} criteria. Thus it is highly desirable to have a clear physical understanding of the correlation and difference between these methods. This is of particular concern for advanced MOSFETs with ultrathin gate insulators and/or undoped SOI bodies for which the classical V_{TH} criterion based on band-bending equal to twice the Fermi potential is inadequate and for which a variety of different criteria have been proposed [8–12]. In this work, we focus on two of them being most physically adequate in such MOSFETs featuring gradual transition from weak to strong inversion, namely:

(i) The maximum of the second derivative of the inversion charge (Q_{inv}) with respect to the gate voltage (V_G), d^2Q_{inv}/dV_G^2, corresponding to the inflection point in the rate of the variation of the inversion charge or surface potential (φ_s) [2,10,13].
(ii) The equality of the drift and diffusion drain current (I_D) components, $I_{diff} = I_{drift}$ [4,9,14].

The criterion of the maximum of d^2Q_{inv}/dV_G^2 lies at the basis of several experimental V_{TH} extraction techniques. Most widely used is the transconductance change method, in which V_{TH} is defined as the gate voltage where the derivative of the transconductance (g_m) in respect to the gate voltage ($dg_m/dV_G \equiv d^2I_D/dV_G^2$) exhibits a maximum [2]. Another method, which relies on the same criterion, is the capacitance derivative method, in which V_{TH} is determined from the position of the maximum of the derivative of the gate-to-channel capacitance C_{GC} [15]. We have recently introduced an alternative method for the V_{TH} extraction based on the same

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criterion, namely, from the position of the minimum of the $d(g_m/I_D)/dV_G$ versus V_G function, which in an ideal MOSFET is shown to coincide with the position of maximum of d^2Q_{inv}/dV_G^2 or minimum of the second derivative of the surface potential $d^2\varphi_s/dV_G^2$ [13]. The $d(g_m/I_D)/dV_G$ method is shown to be much less sensitive to the V_G-dependent mobility [16], as well as to the drain voltage value [17], than the dg_m/dV_G method, and, unlike the dC_{GC}/dV_G method, it can be applied to any small-area devices using standard I_D–V_G measurements.

The equality between I_{diff} and I_{drift} is widely considered to be the underlying physical criterion of the second derivative logarithmic method (SDL) proposed by Aoyama, in which V_{TH} is defined at the minimum of $d^2(\log I_D)/dV_G^2$ [4]. However, noting that

$$\frac{d}{dV_G}\left(\frac{g_m}{I_D}\right)=\frac{d}{dV_G}\left[\frac{1}{I_D}\left(\frac{dI_D}{dV_G}\right)\right]=\frac{d^2\ln I_D}{dV_G^2}=\ln 10\cdot\frac{d^2\log I_D}{dV_G^2}, \tag{1}$$

one can conclude that the gate voltages at which $d(g_m/I_D)/dV_G$ and $d^2(\log I_D)/dV_G^2$ exhibit a minimum should be the same, satisfying the condition $d^2(g_m/I_D)/dV_G^2=0$. Therefore, from the viewpoint of the mathematical procedure, the $d(g_m/I_D)/dV_G$ and SDL methods are identical, although the physical conditions attributed to both methods are different. This raises the question of whether or not these two physical conditions coincide and provide the same V_{TH} values.

In this work, using the unified charge control model (UCCM) [15], we show that, in an ideal MOSFET, the aforementioned two physical conditions correspond to different points on the g_m/I_D curve, that is, they do not coincide. The g_m/I_D methods for the V_{TH} extraction using the criteria of the maximum of d^2Q_{inv}/dV_G^2 and $I_{diff}=I_{drift}$ are considered, and their correlation with other methods is discussed. As our modeling is based on the UCCM, its derivations are expected to be valid for both bulk and SOI MOSFETs. Numerical simulations and experimental data obtained on advanced SOI MOSFETs are used to validate modeling derivations and clarify viability of the g_m/I_D methods.

2. Results of analytical modeling

2.1. Derivation of the analytical expression for g_m/I_D for arbitrary drain voltage and evaluation of the g_m/I_D value at the condition $I_{diff}=I_{drift}$

In our analytical modeling, we assume a long N-channel enhancement-mode MOSFET with zero source potential, $V_S=0$, and ignore quantum and DIBL effects. We also assume a constant mobility along the channel and invariable with gate voltage. According to the Pao–Sah model [18], the drain current I_D accounting for both drift and diffusion components can be expressed as:

$$I_D=qW\mu N_{ch}(y)\frac{dV_{ch}}{dy} \tag{2}$$

where q is the electron charge; W is the channel width; μ is the carrier mobility; y is the distance along the channel; N_{ch} is the inversion carrier density per unit gate area dependent on the position along the channel; V_{ch} is the electrochemical channel potential. Taking into consideration that the current is constant along the channel and integrating along the channel from the source to drain, one can obtain:

$$I_D=q\mu\frac{W}{L}\int_{N_S}^{N_D}N_{ch}\frac{dV_{ch}}{dN_{ch}}dN_{ch} \tag{3}$$

where L is the channel length; N_S and N_D are the inversion carrier densities at the source and drain channel edges, respectively. The term dV_{ch}/dN_{ch} can be calculated from the UCCM Eq. [15]:

$$V_G-V_{TH0}-nV_{ch}=n\phi_T\ln\frac{N_{ch}}{N_0}+\frac{q}{C_{ox}}(N_{ch}-N_0) \tag{4}$$

where V_G is the gate-to-source voltage; V_{TH0} is the threshold voltage at zero drain voltage ($V_D=0$) which in the original UCCM is defined at the maximum of d^2Q_{inv}/dV_G^2 [15]; n is the body factor; $\phi_T=kT/q$ is the thermal potential; C_{ox} is the gate oxide capacitance per unit gate area; and N_0 is the value of the inversion carrier density at $V_G=V_{TH0}$. From (4), assuming V_G to be constant, one obtains:

$$\frac{dV_{ch}}{dN_{ch}}=-\left(\frac{\phi_T}{N_{ch}}+\frac{q}{nC_{ox}}\right) \tag{5}$$

Substituting (5) into (3) and integrating along the channel yields the well-known charge-based current Eq. [19]:

$$I_D=\frac{q\mu W}{L}\cdot\left[\phi_T(N_S-N_D)+\frac{q(N_S^2-N_D^2)}{2nC_{ox}}\right] \tag{6}$$

where the first term in brackets corresponds to the diffusion current and the second to the drift current. From (6) it follows that the condition $I_{diff}=I_{drift}$ is fulfilled when:

$$(N_S+N_D)|_{I_{diff}=I_{drift}}=\frac{2n\phi_TC_{ox}}{q} \tag{7}$$

In what follows we will express g_m/I_D in terms of N_S and N_D, similar to [17]. Differentiating (6) in respect to V_G and rearranging the terms gives:

$$\begin{aligned}\frac{dI_D}{dV_G}&\equiv g_m\\&=\frac{q\mu W}{nL}\cdot\left[\frac{dN_S}{dV_G}\left(n\phi_T+\frac{q}{C_{ox}}N_S\right)-\frac{dN_D}{dV_G}\left(n\phi_T+\frac{q}{C_{ox}}N_D\right)\right]\end{aligned} \tag{8}$$

The $N_S(V_G)$ and $N_D(V_G, V_D)$ dependencies are determined by (4) with V_{ch} equal to $V_S=0$ and V_D, respectively. By differentiating (4) in respect to V_G, we get:

$$\frac{dN_S}{dV_G}=\frac{N_S}{n\phi_T+\frac{q}{C_{ox}}N_S} \tag{9a}$$

$$\frac{dN_D}{dV_G}=\frac{N_D}{n\phi_T+\frac{q}{C_{ox}}N_D} \tag{9b}$$

Substituting (9a) and (9b) in (8) gives:

$$\frac{dI_D}{dV_G}\equiv g_m=\frac{q\mu W}{nL}(N_S-N_D) \tag{10}$$

Next, combining (10) and (6), we obtain a simple expression for g_m/I_D in terms of N_S and N_D:

$$\begin{aligned}\frac{g_m}{I_D}&=\frac{N_S-N_D}{n\phi_T(N_S-N)_D+\frac{q(N_S^2-N_D^2)}{2C_{ox}}}\\&=\frac{1}{n\phi_T+\frac{q}{2C_{ox}}[N_S(V_G)+N_D(V_G,V_D)]}\end{aligned} \tag{11}$$

As follows from (11), the g_m/I_D function takes its maximum value equal to $1/(n\phi_T)$ when N_S and N_D are negligibly small. Substituting (7) into (11) gives the value of g_m/I_D corresponding to the condition $I_{diff}=I_{drift}$ for arbitrary V_D:

$$\left.\frac{g_m}{I_D}\right|_{I_{diff}=I_{drift}}=\frac{1}{2n\phi_T}=\frac{1}{2}\left(\frac{g_m}{I_D}\right)_{\max} \tag{12}$$

Hence, in the ideal long-channel MOSFET, for any V_D, the condition of the equality of the drift and diffusion current components corresponds to the point on the g_m/I_D curve where g_m/I_D is equal to half of its maximum value. Similar result has been previously obtained for the intrinsic symmetric double-gate MOSFET, featuring an ideal subthreshold slope ($n=1$) and operating at very low