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Field controlled RF Graphene FETs with improved high frequency performance

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ABSTRACT

We propose a novel Graphene FET (GFET) with two capacitively coupled field-controlling electrodes (FCEs) at the bottom of the ungated access regions between gate and source/drain. The FCEs could be independently biased to modulate sheet carrier concentration and thereby the resistance in the ungated regions. The reduction of source/drain access resistance results in increased cut off frequency compared to those of conventional GFETs with the same geometry. We studied the DC and improved RF characteristics of the proposed device using both analytical and numerical techniques and compared with the baseline designs.

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1. Introduction

Graphene, a novel electro-optic material consisting of one or a few atomic layers of carbon sheets is considered to be promising for high performance nanoelectronics due to its high carrier concentration, mobility and stability [1,2]. It is a prime candidate for many other electrical and optical applications due to its extremely high thermal conductivity, long phonon mean free path and as a 2D material it could also enable extreme device scaling [3,4]. With its large band structure velocity (1×10^8 cm/s), large saturation velocity (4×10^7 cm/s) and low $1/f$ noise characteristics [5–8], Graphene is particularly attractive for high frequency electronics and numerous groups have reported Graphene analog devices with amplification and phase detection capabilities [9,10]. Moreover, because of strong ambipolar effect and lack of bandgap [2], it is believed to be more suitable for analog applications than it is for digital electronics. Significant progress has been made on Graphene analog devices to achieve good high frequency performance with intrinsic on-chip cut-off frequency up to 300 GHz [11].

It is well known that the source/drain resistances comprising of contact resistance and access resistance impose important set of limitations on the high frequency performance of sub-micrometer FETs. These resistances delay the transition of carriers through the device and reduce the external transconductance leading to a lower drain current. In terms of delay time, reduction of transit delay and parasitic delay ensure high cut-off frequency that can be achieved through shorter gate length and smaller access regions with smaller contact resistances, respectively. Self-aligned fabrication process has been used to reduce the access region length to achieve f_T = 23 GHz for the gate length L_g = 110 nm and ungated regions with the length of 20 nm. [12] However self-aligned process makes fabrication more complex with smaller tolerances.

Reduction of access resistance for enhanced RF performance in III-N HEMTs [13] and in Graphene FETs have been proposed [14,15]. In this paper, rather than reducing the access resistance by minimizing ungated region length or by channel doping, we propose and extensively analyze a novel device structure including 2 field-controlling electrodes (FCEs) capacitively coupled to the ungated regions at the bottom of the device to control the access resistance. Using the proposed device as an amplifier, along with high cut-off frequency due to parasitic delay time minimization, at a fixed DC biasing condition, one would have control over the gain at a certain frequency by tuning the FCE bias. The capacitive coupling technique of the additional contacts ensures mitigation from additional power consumption and the proposed position of FCEs at the bottom of the device would make the fabrication simpler than the top FCE GFETs [16].

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2. Theory

The schematic of a conventional 3-terminal GFET on SiO_2 with the small-signal equivalent circuit overlaid on top is shown in Fig. 1(a).

The gate to source (drain) capacitance C_{gs} (C_{gd}) is composed of both internal and external parts:

$$C_{gd} = C_{gd,i} + C_{gd,ex} \qquad C_{gs} = C_{gs,i} + C_{gs,ex} \tag{1}$$

The external capacitances $C_{gd,ex}$ and $C_{gs,ex}$ are fringe capacitances and independent on gate length whereas the internal capacitances $C_{gd,i}$ and $C_{gs,i}$ directly scale with gate length. If g_m is the intrinsic transconductance, the transit delay, τ_{trans} consisting of intrinsic and extrinsic delay of the device can be expressed as [17,18]:

$$\tau_{trans} = \{(C_{gs,in} + C_{gs,ex}) + (C_{gd,in} + C_{gd,ex})\}/g_m \tag{2}$$

The parasitic time delay due to parasitic resistances and capacitances can be expressed as [17]:

$$\tau_{par} = C_{gd}(R_S + R_D) \cdot [1 + (1 + C_{gs}/C_{gd})g_0/g_m] \tag{3}$$

where $g_0 = 1/R_{SD}$ is the output conductance with R_{SD} is the Drain to Source resistance and R_S and R_D are the source and drain resistance representing the ohmic contact resistance, R_C and source/drain access resistance, R_{acs} in series:

$$R_D = R_S = R_C + (L_{acs}/\mu q n_0 W) \tag{4}$$

here L_{acs} is the access region length (L_{gs} and L_{gd}), μ is the carrier mobility, q is electronic charge, n_0 is the residual carrier density in Graphene and W is the device width. The current gain cut-off frequency f_T is inversely proportional to the total delay time in the device and can be expressed as:

$$1/2\pi f_T = \tau_{trans} + \tau_{par} \tag{5}$$

Thus, summing up all the delay times and rearranging, the f_T of the device can be related to the small signal circuit parameters as follows:

$$f_T = \frac{g_m/(2\pi)}{[C_{gs} + C_{gd}] \cdot [1 + (R_S + R_D)/R_{SD}] + C_{gd} \cdot g_m \cdot (R_S + R_D)} \tag{6}$$

where R_{SD} is the Graphene channel resistance that can be expressed as follows [12]:

$$R_{SD} = L_G/\mu q (n_0^2 + n_g^2)^{1/2} W \tag{7}$$

where n_g is the carrier density due to gate modulation. One needs to minimize the delay times to increase the current gain cut-off frequency.

Fig. 1(b) clearly show that the effect of parasitic time delay τ_{par} becomes more prominent compared to other delays for short channel GFETs. Similar results were obtained for short channel $In_{0.7}Ga_{0.3}As$ HFETs as well [19]. The indispensable minimization of parasitic delay time for GFETs with improved RF performance becomes possible by reducing the source and drain access resistance using FCEs. As proposed, an FCE of length L_{FCE} placed at the access region making two no-FCE regions named $L_{S/D\text{-}FCE}$ and $L_{g\text{-}FCE}$ at the S/D and gate end of each FCE respectively can changes the expression of R_S and R_D as follows:

$$R_S = R_D = 2R_C + \frac{2L_{g\text{-FCE}}}{\mu q n_0 \cdot W} + \frac{2L_{S/D\text{-FCE}}}{\mu q n_0 \cdot W} + \frac{2L_{FCE}}{\mu q (n_0^2 + n_{FCE}^2)^{1/2} W} \tag{8}$$

The resistance of the ungated access regions decreases by the induced carriers n_{FCE} due to FCE modulation which results in a decrement of τ_{par} and increment of f_T.

3. Results and discussion

To validate our simulation method, we selected a baseline conventional GFET with experimental data reported in the literature and replicated its measured DC and RF characteristics [3]. Later to validate our proposed method of improving RF characteristics, we added the FCEs at the bottom of ungated regions of the device and estimated the improvement of f_T over the reported one using both analytical and numerical techniques. The baseline device has CVD grown Graphene channel with electron mobility of $\mu_E = 336\ cm^2/V\,s$ and hole mobility of $\mu_H = 530\ cm^2/V\,s$ on 300 nm SiO_2 with gate length of $L_g = 3\ \mu m$, source/drain access length of $L_{gs}/L_{gd} = 1.5\ \mu m$ and 24 nm thick gate dielectric as shown in Fig. 2(a). We named this long channel low mobility device as GFET-A. From the reported DC characteristics of the device, we extracted the residual carrier (hole) concentration of Graphene as $7.02 \times 10^{12}\ cm^{-2}$. This value of residual carrier concentration leads to an access resistance value of 25.2 Ω for the 1.5 μm long ungated regions on both sides of the gate considering the device width to be 100 μm. We have used physically-based device simulation tool to simulate our device. This type of simulation approximates the operation and transportation of carriers through the structure by applying a set of differential equations including Poisson's Equation, Carrier Continuity Equations and Drift–Diffusion Equation, derived from Maxwell's laws, onto a 2D grid, consisting of a number of grid points called nodes. This way the electrical performance of a device can be modeled in DC, AC or transient modes of operation [20]. The simulated DC and RF characteristics of the baseline device using such a tool with parameters modified for Graphene are presented in Fig. 2(c) which are in good agreement with the reported ones. The extracted f_T and f_{MAX} are 1.0 GHz and 1.2 GHz, respectively.

In the I_d–V_g characteristics of a GFET, the lowest current point is the Dirac point which has the hole dominant region on its left and electron dominant region on right. Though the operating regime of GFETs is user's choice, the total device current on either regime is also supported by the low density residual carriers available at the ungated regions contributing to the source/drain resistance which affects the RF performance.

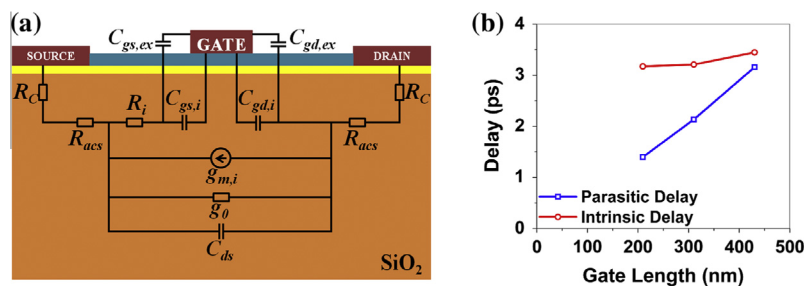

Fig. 1. (a) Schematic of a typical GFET on SiO_2 with small-signal equivalent circuit overlaid on top. (b) Intrinsic and parasitic time delays vs. gate length of GFET reproduced from [17].

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