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Comprehensive study of the statistical variability in a 22 nm fully depleted ultra-thin-body SOI MOSFET

Anis Suhaila Mohd Zain [a,b,*], Stanislav Markov [a], Binjie Cheng [a], Asen Asenov [a,c]

[a] Device Modelling Group, School of Engineering, University of Glasgow, Glasgow G12 8LT, UK
[b] Universiti Teknikal Malaysia Melaka (UTeM), Hang Tuah Jaya, 76 100 Durian Tunggal, Melaka, Malaysia
[c] Gold Standard Simulations Ltd., Rankine Building, Glasgow G12 8LT, UK

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ABSTRACT

A comprehensive study of statistical variability (SV) in scaled, fully-depleted (FD) SOI n-channel MOSFET with a physical gate length of 22 nm is reported. The impact of random discrete dopant (RDF), line edge roughness (LER) and metal gate granularity (MGG) on threshold voltage (V_{TH}), drain-induced-barrier-lowering (DIBL) and on-current (I_{on}) are analyzed both individually and combined together. Results indicate that although MGG is the dominated variability source in the FD-SOI transistor, RDF has critical impact on the on-current variability. Moreover, the combination of RDF and LER can still dramatically modulate short channel effect behavior in the transistor.

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1. Introduction

Statistical variability has been identified as a critical challenge in CMOS scaling, affecting performance, power, and yield of ULSI circuit and system [1,2]. It has far reaching influence on SRAM circuits, requiring careful consideration at device level [3]. The progressive scaling of traditional planar, bulk MOSFETs is reaching its limit due to the very high channel doping concentration, which is needed to control short-channel effects, leading simultaneously to unacceptably high variability in threshold voltage (V_{TH}) due to random dopant fluctuations (RDFs) [4,5]. In this respect, novel aspects of device technology and architecture have been introduced to allow further miniaturization while mitigating variability. For example, the deployment of high permittivity gate stacks, in combination with metal-gates has been elemental in reducing the equivalent oxide thickness (EOT) and attenuating the impact of RDF [6]. However, metal-gate-granularity (MGG) and the associated work-function variability (WFV) continue to have a critical impact on V_{TH}, together with fluctuations in the definition of the gate-edges, known as line edge roughness (LER) [4,7,8]. For the 22 nm technology generation and beyond, devices with fully depleted (FD) channel show better scaling potential owing to superior electrostatic integrity without the need to introduce high doping concentration in the channel, hence with lower RDF-induced V_{TH} fluctuations [9,10]. In fact, fully depleted FD-SOI technology has demonstrated the smallest mismatch coefficient A_{vt}, i.e. smallest standard deviation σV_{TH} [11,12]. However, its overall variability, in terms of DIBL and I_{on} is less studied. The different nature of RDF, MGG and LER affects the dispersion of threshold voltage, on-current (I_{on}) and DIBL in different way, and it was recently shown that RDF in the source/drain extensions (S/D-RDF) is a dominant contributor to I_{on} fluctuations [13,14]. Those variability aspects are explored here, in view of their importance to device and circuit design and performance.

The paper is organized as follows. In Section 2, we describe the macroscopic device template that is used to create an ensemble of microscopically different transistors for simulation of statistical variability. In Section 3 we discuss the impact of each of the principle variability sources individually and in combinations. Two combinations are used, RDF and LER with MGG, and RDF with LER only since a lot of technological effort is devoted to the elimination of WFV in metal-gates adopting metal gate last process [15]. Conclusions are drawn in Section 4.

2. Devices and simulation methodology

The design of the 22 nm template UTB SOI is based on ITRS (2009) requirements and targets low power (LOP) applications, with a supply voltage (V_{dd}) of 0.8 V [16]. The template features 22 nm physical gate length, metal gate and high-*k* dielectric stack with a thin SiO_x interfacial layer ($TiN/HfO_2/SiO_x$) and an effective oxide thickness of 0.9 nm. The buried oxide (BOX) and Si-body thickness (Tsi) are 10 nm and 7 nm respectively. Body/substrate acceptor doping is $1.2 \times 10^{15}/1.0 \times 10^{18}$ cm^{-3}. S/D-extensions donor concentration is 2.0×10^{20} cm^{-3}, with a continuous roll-off

* Corresponding author at: Device Modelling Group, School of Engineering, University of Glasgow, Glasgow G12 8LT, UK.
E-mail address: anis@elec.gla.ac.uk (A.S. Mohd Zain).

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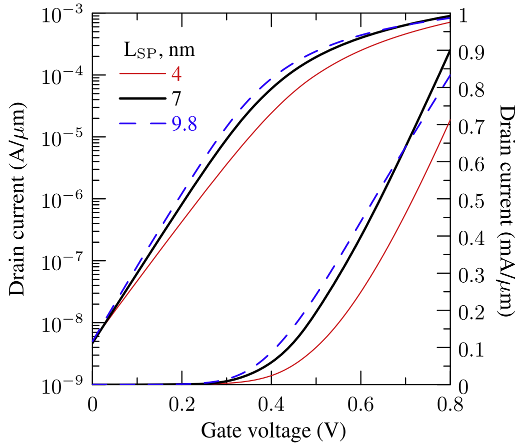

Fig. 1. Transfer characteristics (I_DV_G) of the template FD-SOI device, for three different widths of the spacer between the gate and S/D regions. The optimal design is with 7 nm spacer, which is used throughout this work.

of 2 nm/dec under the spacer and into the channel. For simplicity, vertical gradient of the donor concentration is not considered.

The spacer chosen for this study is 7 nm, which appears to be the optimal value for achieving I_{on} of 0.9 mA/μm with an acceptable DIBL and sub-threshold slope (SS). This is clear from Fig. 1, which compares the transfer characteristics of the template structure at three different widths of the spacer L_{SP}. The gate work-functions are adjusted so that I_{off} is the same (5 nA/μm) for each of the three cases considered. Table 1 summarizes the electrical figures of merit for each case. Note that for the thinnest spacer of 4 nm, the proximity of the drain to the gate dramatically affects short-channel effects, raises SS and DIBL, and actually degrades the drive current, in comparison to thicker spacers. On the contrary, too thick spacer degrades the drive current through the access resistance of the S/D-extensions.

Table 1
Performance versus spacer width at I_{off} = 5 nA/μm.

L_{SP} (nm)	V_{TH} (mV)	I_{on} (mA/μm)	SS (mV/dec)	DIBL (mV/V)
4	239	0.71	103	173
7	205	0.90	88	106
9	192	0.83	82	80

Based on the selected template, we perform statistical simulations on 1000-device ensembles of microscopically different transistors, by using the 3D density-gradient-corrected drift–diffusion simulator GARAND [17]. Ensembles differ in the included sources of statistical variability: RDF, LER, MGG, and combination of these. The relevant modeling parameters for LER are $3\sigma = 2$ nm (slightly below 10% of L_G) and a correlation length $\lambda = 25$ nm [16,18]. TiN MGG leads to two work-functions differing by 0.2 V, probability of 0.4/0.6 for the higher/lower WF, and an average grain-size $\varnothing = 5$ nm [7,19]. RDF is introduced using a rejection technique based on the continuous doping profile of the template, as in [14]. In this way the penetration of donors, as well as the occasional occurrence of an acceptor in the channel of the transistor due to the finite implant concentration there, are realistically modeled. Threshold voltage V_{TH} is defined as the gate voltage necessary to obtain 5 μA/μm drain current.

3. Statistical variability

3.1. A. Qualitative analysis

In this section we systematically compare the impact of RDF, LER and MGG on saturation V_{TH} and I_{on}, and on DIBL. In order to anticipate and understand that impact, we first look at the microscopic effects inside a device, due to each source of variability. In Fig. 2 we illustrate the electron potential landscape and three iso-electron-concentration surfaces in the body of the device for

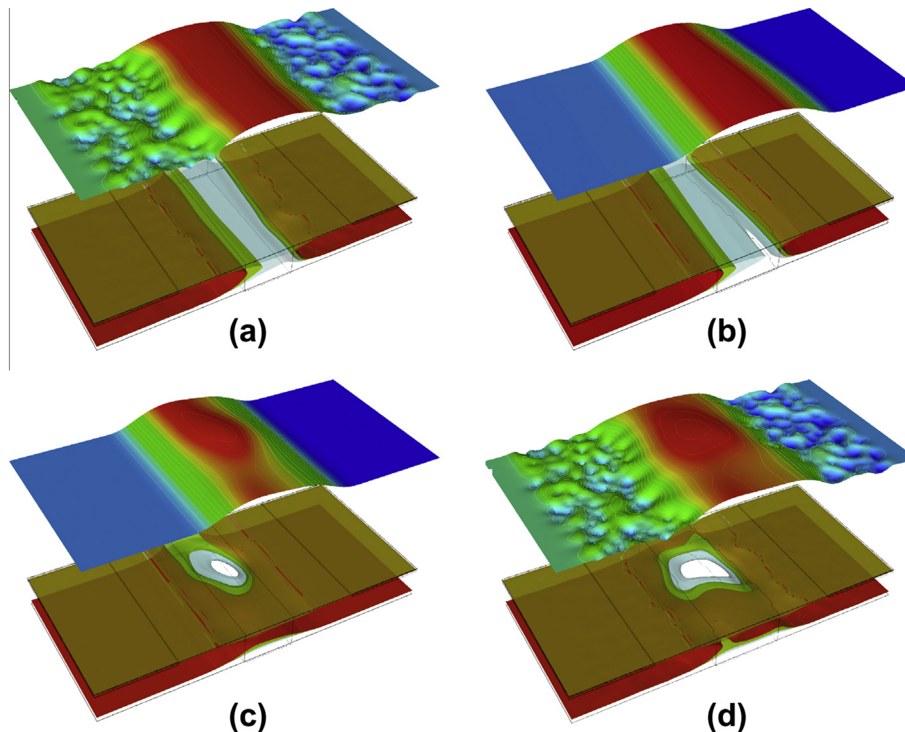

Fig. 2. Conduction band landscape and three iso-electron concentration surfaces in the body of the device, in the presence of RDF (a), LER (b), MGG (c) on their own, and in combination (d).

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