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Characterizations of polycrystalline silicon nanowire thin-film transistors enhanced by metal-induced lateral crystallization

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ABSTRACT

In this paper, we present a comprehensive study on the effects of layout design and re-crystallization temperature on the material and electrical characteristics of polycrystalline silicon thin-film transistors (poly-Si TFTs) with metal-induced lateral crystallized (MILC) nanowire (NW) channels. It is found that the off-state leakage current shows strong dependence on the arrangement of MILC seeding windows, while the number of smaller solid-phase-crystallized (SPC) grains in the channel is reduced by lowering the re-crystallization temperature, thus improving the on-state behavior. Moreover, owing to the spatial confinement for MILC fronts, small cross-section of the NW channel would result in little lateral crystallization, and thus retarding the enhancement in performance of MILC NW devices.

1. Introduction

Field-effect transistors (FETs) constructed with polycrystalline silicon nanowire (poly-Si NW) channels recently have attracted enormous attentions for a number of promising applications, such as high-performance thin-film transistors (TFTs) [1,2], real-time detection biosensors [3,4], and flash memory devices [5,6]. This is mainly attributed to the inherent properties of NW's small body and high surface-to-volume ratio, and thus the electrostatic states in the NW channel are sensitive to the surface conditions exerted by conventional solid gates or biochemical gates. Besides, the amount of defects contained in the tiny poly-Si NW structure is comparatively reduced, leading to lower leakage current and higher carrier mobility [7]. Moreover, the mobility of carriers in poly-Si greatly depends on both grain size and intra-grain micro-structural defects. In view of this, metal-induced lateral crystallization (MILC) technique presents a low-cost and promising approach to grow large-area poly-Si films with enhanced crystallinity at lower temperatures (below 600 °C) by using metal silicides as the crystallization agent [8–10]. It has been reported that high-performance poly-Si TFTs can be realized owing to the MILC longitudinal grains largely parallel to the drain current, hence yielding higher mobility [11,12]. Lately, we have successfully developed a novel scheme for fabricating poly-Si NW TFTs by utilizing MILC technique to achieve superior crystalline properties and electrical behaviors [2,13]. The results evidently reveal that the NW channels enhanced by MILC approach are suitable for high-performance device applications. We believe this is because the large and needle-like MILC grains can be formed in parallel to the NW channel direction, and therefore it is feasible to obtain the NW with nearly monocrystalline structure [14]. However, in the implementation of MILC process, our preliminary data seemed to suggest that the arrangement of MILC seeding windows and NW dimensions play an important role in affecting the resulted film quality and device performance [2]. So in this study, several parameters including different MILC seeding window offset (i.e., spacing between the window and the channel region, as shown in Fig. 1), dimensions of NW channels and annealing conditions, were designed and thoroughly investigated for better comprehension of MILC mechanism in the NW regime.

2. Device structure and experiments

The proposed MILC NW device features the source/drain (S/D) regions and NW channels across and abutting against the side-gate, respectively, as illustrated in Fig. 1. Briefly, the fabrication process started with the formation of the n^+-poly-Si gate on an oxidized Si substrate. Then, a 40 nm-thick tetraethyl-orthosilicate (TEOS) oxide serving as the gate oxide was deposited in a low-pressure chemical vapor deposition (LPCVD) system, followed by the deposition of a 100 nm-thick amorphous Si (a-Si) layer. Afterwards, S/D dopants were implanted with P_{31}^+ ion beam with a dose of 1×10^{15} cm^{-2} at 15 keV. Subsequently, S/D photoresist

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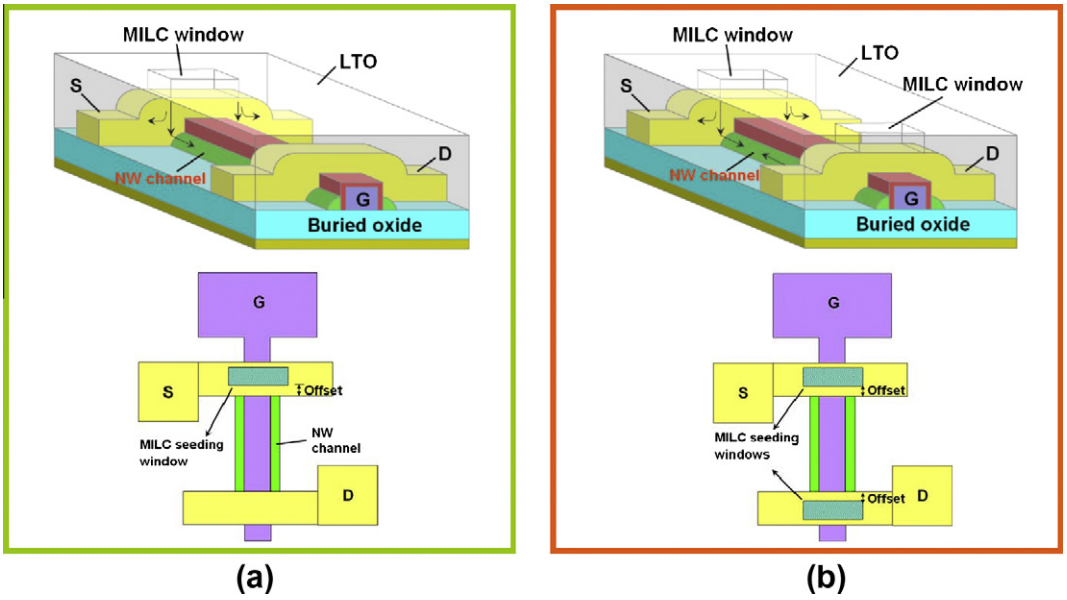

Fig. 1. Side and top views of the MILC devices with (a) MIUC and (b) MIBC configurations. Offset is defined as the spacing between the MILC seeding window and NW channel region.

patterns were generated using a g-line stepper and the regions were subsequently patterned by an anisotropic dry etching step using HBr/Cl_2 gases. During the etching process, the NW channels were simultaneously formed on the sidewalls of the gate structure, similar to the formation of sidewall spacers employed in standard CMOS manufacturing. Note that the NW channels were accomplished in a self-aligned manner with respect to the S/D and remained undoped because the aforementioned implant was done at a low energy so the implanted dopants do not reach the channel. A 100 nm-thick low-temperature oxide (LTO) was then deposited by a plasma-enhanced (PE) CVD. For MILC purpose, the seeding windows were opened in the LTO layer. In this work, two splits of samples were exploited, as illustrated in Fig. 1. In one split, denoted as the metal-induced unilateral crystallization (MIUC) split (Fig. 1a), only a single window was opened on the source region. Here the source region is defined as the terminal that serves as the grounded source during normal device characterization. In the other split, two windows symmetric to the channel center were opened on both the source and drain regions, and denoted as the metal-induced bilateral crystallization (MIBC) split (Fig. 1b). After opening the seeding windows, a 5 nm-thick Ni layer was deposited to serve as the seeding layer. The lateral crystallization was carried out at 550 °C in N_2 ambient for 21 h, unless mentioned otherwise. The arrows shown in Fig. 1 indicate the crystallization paths. Next, the unreacted Ni was disposed off in an H_2SO_4/H_2O_2 solution. Afterwards, an additional annealing step at 600 °C for 6 h was performed for the purpose of S/D dopant activation. After depositing a 200 nm passivation oxide layer and opening contact holes, a standard metallization step was performed to complete the device fabrication. It is worth noting that the overall process flow is quite simple and straightforward.

3. Results and discussion

3.1. Material properties of MILC NWs

Fig. 2 shows the top-view scanning electron microscopic (SEM) image of an MILC sample taken near the seeding window. It can be seen that the large needle-like Si grains protrude from the MILC seeding window, and the width of them reaches 90 nm. Generally,

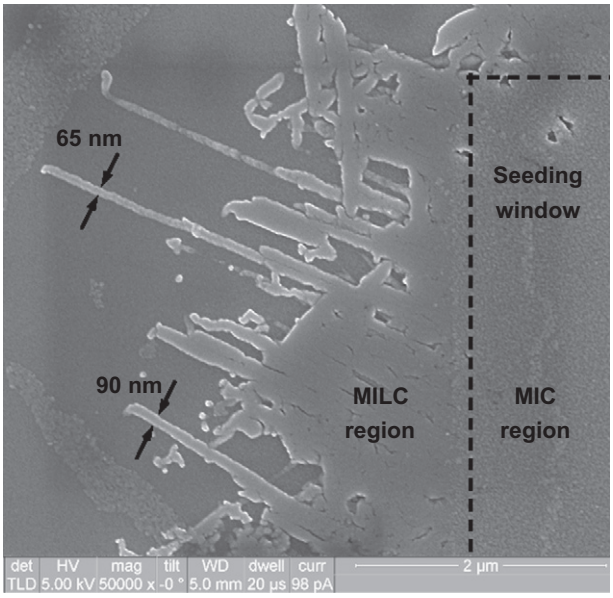

Fig. 2. Top-view SEM image of an MILC poly-Si sample near the seeding window. Secco etching was used to remove most of amorphous Si.

the size of NW fabricated in our study is deliberately controlled to be smaller than 50 nm in width as shown in Fig. 3. As a result, once the NW feature size is shrunk to less than the lateral size of the needle grain, it becomes feasible to achieve single-crystal NW structure. Fig. 4a shows the migration of a $NiSi_2$ precipitate with size of 50 nm by 10 nm in the NW, leaving behind the needle-like Si crystallite. In this case, single-crystalline Si property is thus obtained. For better understanding of detailed crystalline property in the NW, Fig. 4b displays the plan-view transmission electron microscopic (TEM) image of an MILC sample near the seeding window on the test structure. The NW shows long and large grains in it. Near the seeding window, the length of the single-crystal Si grain is found to be about 1 µm. The electron diffraction pattern at the circled region further verifies that this visible Si NW exhibits monocrystalline structure with ⟨1 1 0⟩ orientation. However, the