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High-performance vertically stacked bottom-gate and top-gate polycrystalline silicon thin-film transistors for three-dimensional integrated circuits

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ABSTRACT

The three-dimensional CMOS inverter with top-gate (TG) poly-Si thin film transistors (TFTs) vertically stacked on the bottom-gate (BG) poly-Si TFTs have been proposed to achieve high-performance characteristics via excimer laser crystallization (ELC) for the first time. Under an appropriate laser irradiation energy density, the silicon grain growth could be controlled from the sidewalls of the bottom-gate structure and thus the high-quality laterally grown poly-Si film with single perpendicular grain boundary in the channel would be formed for the BG TFTs. In addition, a simple ELC method was also utilized to the top-layered poly-Si film for TG TFTs as compared with solid-state-crystallized (SPC) ones. As a result, the field-effect mobilities of the proposed n-type BG and p-type TG TFTs could be significantly increased to be 390 and 131 cm^2/V s, respectively, in contrast to 32.3 and 14.7 cm^2/V s for the SPC ones, accordingly. Furthermore, such three-dimensional (3-D) TFT have also been employed to demonstrate the inverter devices and is suitable for future 3-D ICs as well as system-on-panel applications.

1. Introduction

In the past years, shrinkage of the device dimension was one of the technologies to increase transistor density and improve circuit performance on integrated circuits [1,2]. However, the device dimension might not be shrunk infinitely. Therefore, the scaling-down technologies to increase the transistor density might approach the scaling limitation [3,4]. Moreover, with decreasing the feature size, the importance of interconnect delay increases [5].

Owing to the scaling limit and the increasing domination of the interconnects, a further increase of device density and reduction of delay would depend on the three-dimensional integration technology [6–8]. Vertically stacked multifloor structure has been considered as one of the ultimate three-dimensional integrated circuits (3-D ICs) in future [9]. From the viewpoint of reduction of interconnect delay, the connection of the function blocks could be replaced by the shorter and vertical interconnects for 2-layer devices. Therefore, the interconnect delay of 3-D ICs would be reduced as compared with 2-D ICs [6]. In the perspective of reduction of chip area, it has reported that a 50% area reduction could be attained by employing two stacked device layers over the standard 2-D IC structure [10]. Furthermore, the process could be simplified by means of fabricating only one type of device instead of complementary ones on each layer [11].

One of the main challenges to implement 3-D stacked transistors was the thermal budget. The high temperature processing of second layer of devices and beyond might be a threat to cause dopant diffusion in the lower layers of devices [12]. Another obstacles of developing 3-D stacked device layer technology was to obtain high quality silicon layer for the multi-level purpose [13], for example, solid-phase crystallization [14], selective epitaxial growth and epitaxial lateral growth of silicon [15], crystallization of amorphous silicon using Ge [16], metal induced lateral crystallization [12], etc. Some of these methods might cause poor film quality and metal contamination as well as suffer from complicated process and high thermal budget [17,18].

One promising approach for achieving high-quality silicon grains with low thermal budget was to utilize ELC [19]. Under the laser annealing conditions near the super lateral growth (SLG) regime, the large grains can be obtained for high-performance poly-Si TFTs. In addition, various poly-Si grain enhancement technologies with ELC have been proposed to further improve the uniformity and performance of poly-Si TFTs, including the a-Si spacer [20], recessed-channel structure [21], and so on [22–29]. However, some of them might need complex process or requiring complicated laser annealing systems.

A simple structure of bottom-gate (BG) TFTs vertically stacked with top-gate (TG) TFTs possessing low thermal budget and easy fabrication procedure was proposed to attain high-performance 3-D ICs via ELC. Consequently, the bottom-layered BG poly-Si TFTs with single perpendicular grain boundary in the channel would demonstrate high-performance electrical characteristics.

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Furthermore, the complementary 3-D poly-Si invertors with p-type top-gate (TG) TFTs stacked on the n-type bottom-gate (BG) ones were also demonstrated with good characteristics for the system-on-panel and 3-D integrated CMOS applications.

2. Device fabrication

Fig. 1 displays the key fabrication steps for the proposed 3-D CMOS inverter with BG and TG poly-Si TFTs crystallized via ELC. At first, an 100-nm-thick phosphorus-doped polysilicon layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C on oxidized silicon wafers. After definition the bottom-layer bottom gate electrode, an 100-nm-thick tetraethyl orthosilicate (TEOS) gate oxide layer and an 100-nm-thick a-Si layer were deposited by LPCVD. Then, the samples were performed by a KrF excimer laser irradiation ($\lambda = 248$ nm) at room temperature and the number of laser shots per area was 20 (i.e., 95% overlapping). After ELC, the poly-Si active layers were etched to define the bottom-layered active channel region. Next, a phosphorus ion implantation with a dose of 5×10^{15} cm^{-2} was carried out to form the n-type bottom-layered source and drain regions. After the deposition of a TEOS separation oxide, an 100-nm-thick a-Si layer were deposited by LPCVD and irradiated by the KrF excimer laser. Next, the poly-Si active layers were etched to define the top-layered active channel region. After that, an 100-nm-thick TEOS gate oxide layer and an 100-nm-thick in situ doped phosphorus poly-Si layer were deposited. The poly-Si gate and gate oxide were etched to form top-layered top-gate region. Then, a boron ion implantation with a dose of 5×10^{15} cm^{-2} was carried out to form the p-type top-layered source and drain regions. Afterwards, a TEOS passivation oxide layer was deposited, and the dopant activation was performed by thermal annealing at 600 °C for 10 h. Finally, contact hole opening, metallization, and sintering process were carried out to complete the fabrication of the 3-D BG and TG TFTs. For the comparison, the conventional SPC TG poly-Si TFTs were also fabricated.

3. Results and discussion

The plane-view scanning electron microscopy (SEM) photographs, as shown in Figs. 2 and 3, verify the grain boundaries in the channels for the bottom-layered and top-layered devices. For the bottom-layered ELC BG poly-Si thin film, Fig. 2a and b show the SEM images of the films without and with optimum laser irradiation energy density after Secco etching, respectively. It was observed that the silicon grains uniformly existed in the channel region and only one perpendicular grain boundary was formed in the center of the channel under optimum laser irradiation energy density of 460 mJ/cm^2, as illustrated in Fig. 2b. However, Fig. 2a displays the poly-Si thin film having many small grains without optimum laser irradiation energy density of 420 mJ/cm^2. When the excimer laser irradiation is irradiated on the a-Si thin film, the optimum laser energy density is controlled to completely melt the thin channel region of a-Si film and partially melt the thick region of a-Si near the sidewalls of the bottom gate. A lot of un-melting solid seeds remain near the sidewalls of bottom-gate electrode. Consequently, a lateral temperature gradient can be produced between the thin channel and thick sidewalls of a-Si thin film, and the grains will grow laterally from the sidewalls to towards the channel region. Therefore, the lateral growth can be artificially

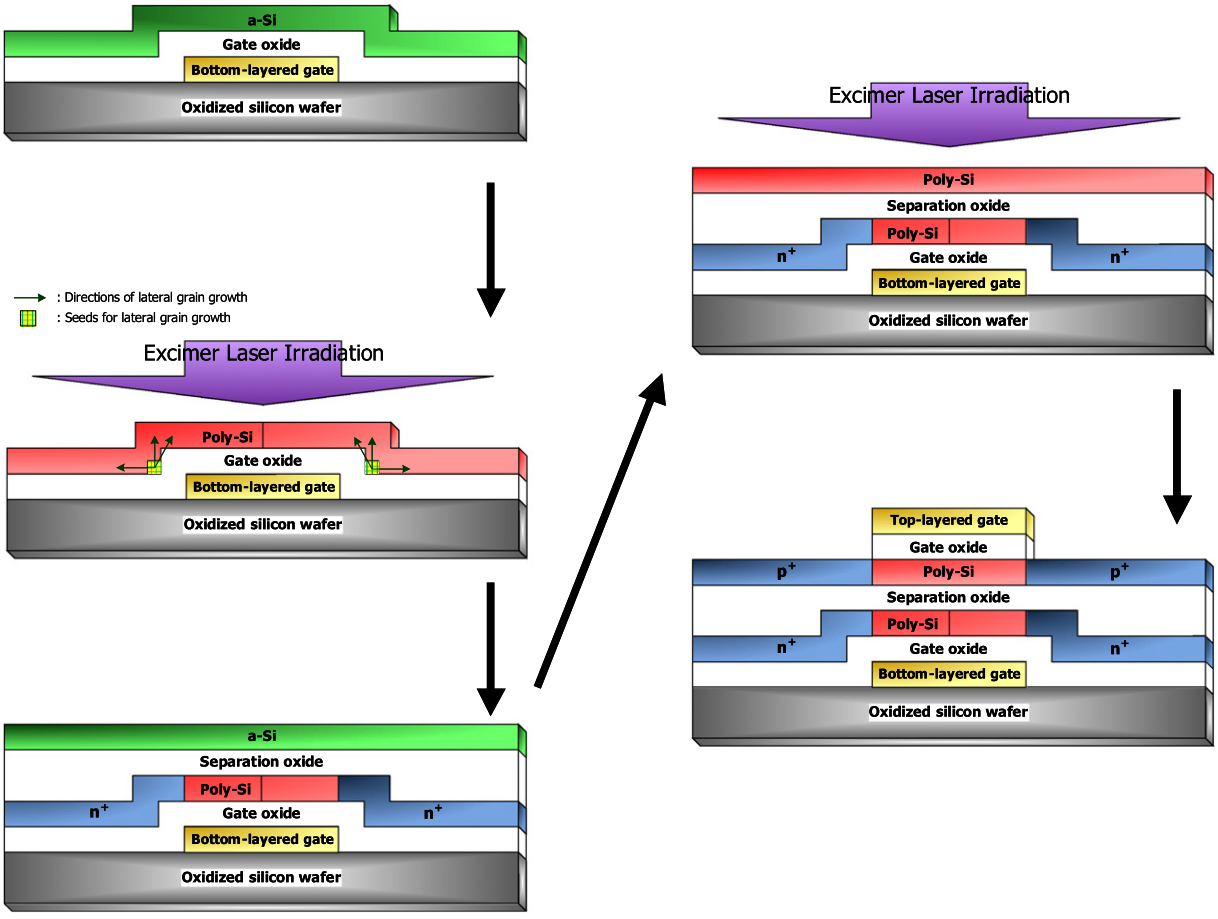

Fig. 1. Schematic diagrams of the key-process procedures of the proposed 3-D bottom-gate (BG) and top-gate (TG) poly-Si TFTs crystallized with ELC.