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Letter

Extraction of trap densities in poly-Si thin-film transistors fabricated by solid-phase crystallization and dependence on temperature and time of post annealing

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ABSTRACT

Trap densities in poly-Si thin-film transistors fabricated by solid-phase crystallization have been extracted by measuring low-frequency capacitance–voltage characteristics and using a novel extraction algorithm. Moreover, the dependence of the trap densities on temperature and time of post annealing has been evaluated. It is found that the trap densities are flatly distributed and very roughly 10^{18} cm^{-3} eV^{-1} near the midgap and become tail states near the conduction band. Furthermore, the trap densities can be reduced by increasing the temperature and time of the post annealing. This is brought by the extinction of crystal defects generated during the solid-phase crystallization.

High-temperature poly-Si thin-film transistors (HTPS TFTs) are matured devices as key components in data projectors using liquid–crystal displays and also promising devices as view finders in digital cameras, etc. [1–6]. The outstanding advantage is that the reliability under severe bias and temperature stress is higher than those of low-temperature poly-Si TFTs (LTPS TFTs) and amorphous-Si TFTs. However, the transistor performances such as carrier mobilities are not so excellent in comparison with LTPS TFTs. Therefore, we think that there is much room for improvement in HTPS TFTs.

Trap densities in channel layers (D_{if}) are some of the main determinants of transistor performances. Therefore, it is important to extract D_{if} in order to diagnose fabrication processes, improve transistor performances, etc. To date, D_{if} in HTPS TFTs have been also reported in some papers [7–9]. Recently, we have developed an extraction technique of D_{if} by measuring low-frequency (low-*f*) capacitance–voltage (*C*–*V*) characteristics and using a novel extraction algorithm [10]. Although the extraction technique has been first applied to oxide–semiconductor TFTs, it can be also applied to HTPS TFTs. The unique merit is that the charge densities in HTPS TFTs are directly counted from the transistor characteristics and no mobility model is necessary unlike the conventional techniques.

In this research, D_{if} in poly-Si TFTs fabricated by solid-phase crystallization (SPC TFTs) has been extracted by measuring low-*f* *C*–*V* characteristics and using a novel extraction algorithm. Moreover, the dependence of D_{if} on temperature and time of post annealing has been evaluated. It is found that D_{if} is flatly distributed and very roughly 10^{18} cm^{-3} eV^{-1} near the midgap and becomes tail states near the conduction band (Ec). Furthermore, D_{if} can be reduced by increasing the temperature and time of the post annealing. This is brought by the extinction of crystal defects generated during the SPC.

First, the top-gate, coplanar and n-type SPC TFTs are fabricated [11,12]. An amorphous Si film is deposited on a quartz substrate using low-pressure chemical vapor deposition (LPCVD) of SiH_4 and crystallized using furnace annealing in N_2 ambient to form a poly-Si film without any intentional doping, which leads fully depletion mode in transistor behavior. A SiO_2 film is grown using thermal oxidation in O_2 ambient and deposited using chemical vapor deposition (CVD) to form a gate insulator film. The poly-Si film is upgraded using post annealing either at 1000 °C for 1 h, at 1050 °C for 1 h, at 1000 °C for 2 h or at 1050 °C for 1 h + at 1000 °C for 1 h. Phosphorus ions and boron ions are implanted, whose dose densities are 2×10^{15} cm^{-2} and 1×10^{15} cm^{-2}, respectively, and activated using furnace annealing to form source and drain regions. The thicknesses of the poly-Si and gate insulator films are 54.0 nm and 33.7 nm, respectively. The gate width and length are 100 μm and 1 μm, respectively.

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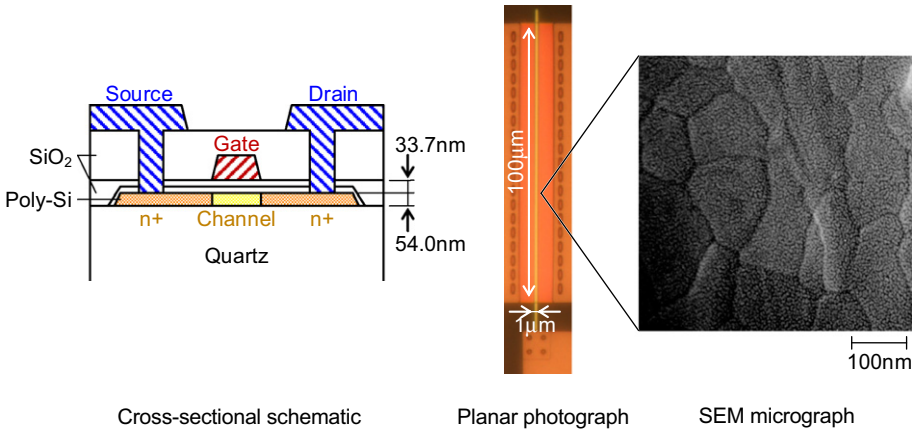

Fig. 1. Structure of the TFT fabricated by solid-phase crystallization (SPC). The grain size is so small that D_{if} can be assumed uniform in the poly-Si films. The grains and grain boundaries do not change their shapes and locations once the poly-Si films are formed using the SPC even after the post annealing around 1000 °C.

Fig. 1 shows the structure of the SPC TFT. Here, the cross-sectional schematic, planar photograph and SEM micrograph of the poly-Si film are shown. It is well known that poly-Si films formed using the SPC have many crystal defects in the grains [7–9]. The grain size is so small that D_{if} can be assumed uniform in the poly-Si films. Moreover, it is reported that the grains and grain boundaries do not change their shapes and locations once the poly-Si films are formed using the SPC even after the post annealing around 1000 °C [11].

Next, the low-f C–V characteristics are measured. The gate voltage (V_{gs}) is applied to the gate terminal with overlapping a small AC signal, the source and drain terminals are connected, the electric current flowing through the source–drain terminal is detected, and the capacitance between the gate and source–drain terminals ($C_{g(s+d)}$) is measured. Since this extraction technique needs that the measurement frequency (f) is extremely low in order to get thermal equilibrium conditions in which the spatial profiles of the electric potential and carrier densities in the channel layers are uniform and the trapping ratio of the trap states is saturated, the C–V measurement system is highly customized using a lock-in amplifier, precision voltage source, low-noise current–voltage amplifier, etc. [13].

Fig. 2 shows the dependence of the C–V characteristics on f. Here, for the high-f and negative V_{gs}, although the hole carriers are accumulated in the channel layer, since they cannot be easily transferred beyond the p/n junction at the source and drain regions, $C_{g(s+d)}$ is small. As f decreases, since time is enough for the hole carriers to be transferred, $C_{g(s+d)}$ increases. On the contrary, for the positive V_{gs}, since the electron carriers are accumulated and can be easily transferred, $C_{g(s+d)}$ is always large. As shown in Fig. 2, in this case, since the C–V characteristic at 0.5 Hz is about the same as that at 1 Hz, f should be at most 1 Hz, and the C–V characteristic at 1 Hz is used in the following contents. Such a low-f C–V characteristic of $C_{g(s+d)}$ as small as 100 fF at f as low as 1 Hz can be measured because the C–V measurement system is highly customized as written above.

Fig. 3 shows the dependence of the C–V characteristics on the temperature and time of the post annealing. Here, the C–V characteristics of the n-type TFTs at 1 Hz are plotted. The I–V characteristics of the n-type and p-type TFTs are also plotted in order to determine the intersection voltage (V_0) used in the following equations. Since the reliability is high as written above, no hysteresis appears and no degradation occurs in these measurement conditions, which are not shown here. D_{if} from the midgap to the Ec are extracted from the C–V characteristic above V_0. It is notable that there are local minima just above V_0, which is discussed in the following contents.

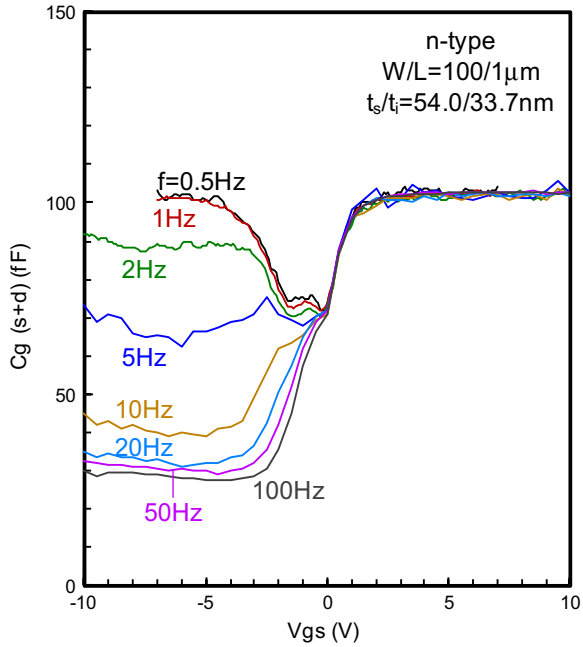

Fig. 2. Dependence of the C–V characteristics on f. In this case, since the C–V characteristic at 0.5 Hz is about the same as that at 1 Hz, f should be at most 1 Hz, and the C–V characteristic at 1 Hz is used in the following contents.

Finally, D_{if} is extracted [10]. First, the surface potential (ϕ_s) is calculated from the C–V characteristic by applying $Q = CV$ to the gate insulator, differentiating it by V_{gs}, transforming it and integrating it by V_{gs}

$$Q = C_i(V_{gs} - \phi_s) \tag{1}$$

$$\phi_s = \int_{V_0}^{V_{gs}} (1 - C_{g(s+d)}/C_i)\, dV_{gs} \tag{2}$$

Here, C_i and $C_{g(s+d)}$ are the geometrical capacitance of the gate insulator and measured capacitance in the low-f C–V characteristic, respectively, and V_0 is the origin voltage at which $\phi_s = 0$. By substituting $C_{g(s+d)}$ into Eq. (2), ϕ_s is calculated for each V_{gs}. Furthermore, the surface potential gradient in the channel layer ($(\partial\phi/\partial x)_s$) is calculated by applying Gauss's law to the insulator interface.

$$(\partial\phi/\partial x)_s = (\varepsilon_i/\varepsilon_s)(V_{gs} - \phi_s)/t_i \tag{3}$$