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Influence of layout design and on-wafer heatspreaders on the thermal behavior of fully-isolated bipolar transistors: Part I – Static analysis

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ABSTRACT

The impact of layout parameters on the steady-state thermal behavior of bipolar junction transistors (BJTs) with full dielectric isolation is extensively analyzed by accurate DC measurements and 3-D numerical simulations. The influence of the aspect ratio of the emitter stripe, as well as the consequences of device scaling, are investigated from a thermal viewpoint. Furthermore, the beneficial effect of implementing aluminum nitride (AlN) thin-film heatspreaders is examined. It is shown that the silicon area surrounding the heat source, as well as the distance to high-thermal-conductivity regions, can have a significant impact on the thermal behavior. A recently proposed scaling rule for the thermal resistance – fully compatible with advanced transistor models – is successfully applied to a series of test BJT structures provided that a simple parameter optimization is carried out. Based on this, some generally applicable guidelines are given to effectively downscale fully-isolated bipolar transistors without significantly worsening the thermal issues.

1. Introduction

In the semiconductor industry, the continuous trends toward miniaturization along with device integration and performance demands are all elements that constantly push research toward more severe isolation schemes. Particularly, the use of silicon-on-insulator (SOI) substrates and trench isolation produces clear improvements in terms of reduced electrical parasitics and cross-talk via the substrate, thus increasing the speed of RF devices and circuits. On the other hand, the low thermal conductivity of most materials used to electrically insulate the devices enhances the thermal issues that in the close future may impose a limit on the current density of high-speed transistors [1]. The ultimate solution for reducing electrical parasitics is given by the silicon-on-glass (SOG) technology where the lossy silicon substrate is replaced by a dielectric (i.e., glass) [2], as shown in Fig. 1, which illustrates three different isolation schemes, namely, a standard junction-isolated bulk-silicon device, a trench-isolated transistor on SOI, and a SOG device. The conflict between electrical and thermal performance is pushed to the extreme in the latter situation (Fig. 1c), where bipolar transistors are characterized by a thermal resistance that can be two orders of magnitude higher than comparable bulk-silicon transistors (Fig. 1a). To quantify the proposed relationships, the self-heating thermal resistances of the basic devices shown in Fig. 1 are estimated by means of 3-D thermal-only numerical simulations, the details of which are given in the following section.

Only a few papers have been published that analyze the thermal behavior of fully-isolated bipolar transistors fabricated on conventional silicon substrates [3–6]. In all these works, the structure under analysis is comprised of an "island" (sometimes referred to as "tub") surrounded by an insulating trench and buried oxide, and embedded in the silicon substrate. In particular, an effort is made in [3] to analytically describe the thermal response of vertical BJTs with the aid of measurements and numerical simulations; in [4], the thermal resistance of the devices is estimated by considering a combination of individual thermal resistances, each of which is

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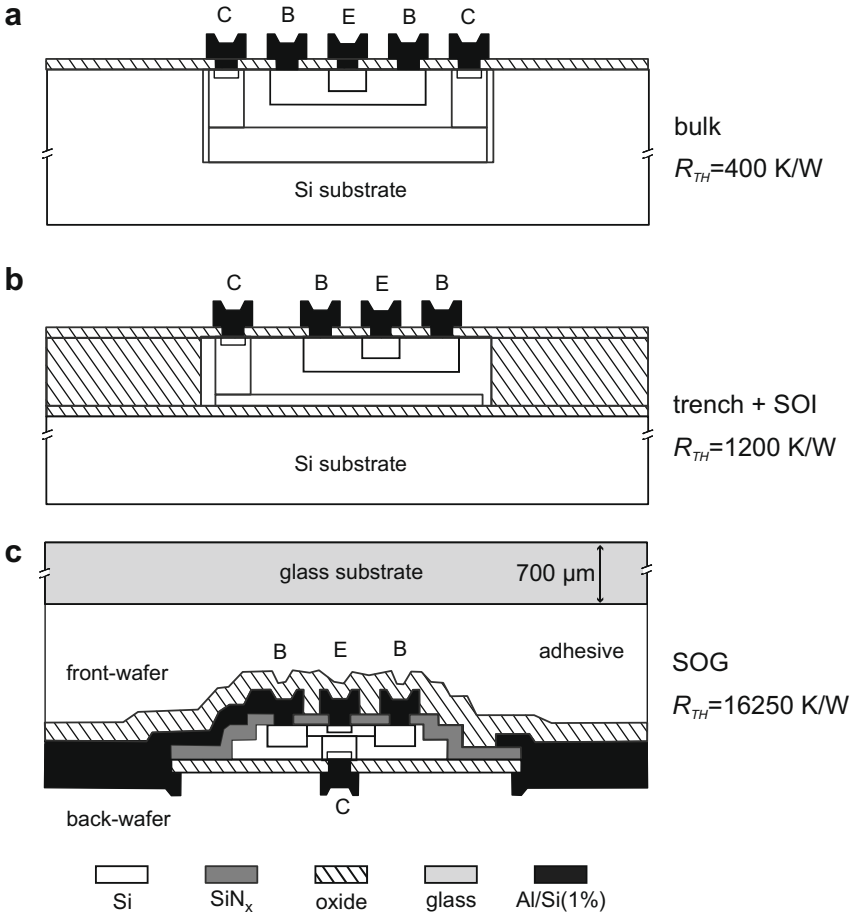

Fig. 1. Schematic cross-sections of bipolar transistors with various isolation schemes: (a) conventional bulk-silicon technology, (b) trench-isolated device on a SOI substrate, and (c) SOG BJT. The numerically-evaluated thermal resistances refer to a device with 1×20 μm^2 emitter area. For (b) and (c), S_1 = 4 μm and S_2 = 14 μm, where S_1 and S_2 are the distances between the edges of the emitter stripe and trench sidewalls, as illustrated in Fig. 2, and the buried oxide layer is 0.4-μm thick.

associated with a specific heat path; in [5], the behavior of the thermal resistance of SiGe heterojunction bipolar transistors (HBTs) is experimentally analyzed as a function of silicon island area; in [6], a parametric analysis of the steady-state thermal behavior of trench-isolated SOI BJTs is carried out through an analytical model supported by a finite-element-method (FEM) analysis. However, none of these investigations cover the case of BJTs fabricated in SOG technology [2], where the low heat-transfer capability of the glass substrate, as well as of all other materials surrounding the silicon island, significantly affects the nature of the heat propagation. Although the analysis of the thermal behavior of SOG BJTs has been the subject of various works (e.g., [7–10]), to date no attempts have been made to clarify the impact of layout parameters on the thermal resistance of such devices.

In Part I of this work, the aim is to supply design guidelines based on a wide experimental and numerical analysis of a variety of SOG test structures operated under steady-state conditions. This study is then extended to treat the dynamic case in Part II [11]. Also investigated is the thermal behavior of state-of-the-art SOG devices that make use of AlN heatspreaders in order to reduce the thermal resistance and guarantee more reliable circuit integration [12]. In Section 2, the test structures and the implementation of AlN in silicon technology are discussed along with the measurement techniques and the 3-D thermal simulation strategy employed for evaluating the thermal resistance. The experimental and simulation results are illustrated in Section 3, which also shows that a scalable model recently proposed in the literature can be employed to accurately predict the increase in thermal resistance with downscaling for both AlN-free and AlN-cooled SOG BJTs. Finally, conclusions are drawn in Section 4.

2. Experimental material and simulation approach

2.1. Test structures

All the experiments are conducted on BJTs fabricated in SOG technology within a 0.94-μm-thick silicon island. In order to study the influence of all the geometrical parameters, several structures with different layouts (i.e., different areas and aspect ratios of the emitter stripe, and distances between emitter stripe and trench) are analyzed. A schematic illustration of the top-view of the devices, with the nomenclature used throughout this manuscript, is depicted in Fig. 2, and a description of the devices under test is given in Table 1.

The measurements are performed on a Cascade probing station equipped with a thermo-chuck and the electrical signals are handled with an Agilent 4156C parameter analyzer. The base–emitter voltage V_{BE} as a function of the base–emitter junction temperature T_j was obtained by measurements performed on bulk-silicon transistors (electrically identical to SOG devices) at various baseplate (i.e., thermo-chuck) temperatures T_B under isothermal (i.e., pulsed) conditions in a wide collector current range (see also Part II [11]).