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Analysis of subthreshold conduction in short-channel recessed source/drain UTB SOI MOSFETs

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ABSTRACT

The subthreshold conduction regime in short-channel recessed source/drain (ReS/D) ultra-thin body (UTB) silicon-on-insulator (SOI) MOSFETs is studied. A physics-based model for the subthreshold slope of ReS/D UTB SOI MOSFETs is developed, based on an analytical solution of 2-D Poisson's equation for the front-gate and back-gate potential distributions. In order to verify the accuracy of the model, the calculated subthreshold slope values are compared with the results obtained by Medici 2-D numerical device simulator over a wide range of different device structures, and very good agreement is obtained down to channel lengths of sub-30 nm. The model is given in explicit form without any fitting parameters and requires no iterative calculation, thus making it ideally suitable for fast prediction and evaluation of device design criteria for optimal scaling of the ReS/D UTB SOI MOSFETs.

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1. Introduction

A fully-depleted silicon-on-insulator (SOI) MOSFET is one of the most promising device architectures as an alternative technology to conventional bulk CMOS, since it allows excellent control of short-channel effects (SCEs) [1–3]. The active part of the fully-depleted SOI MOSFET is in the ultra-thin silicon layer and the buried-oxide underneath suppresses the SCEs. However, short-channel ultra-thin body (UTB) SOI MOSFETs suffer from high parasitic source/drain series resistance caused by the ultra-thin source and drain regions required for adequate device performance [4,5]. Therefore, recessed source/drain (ReS/D) UTB SOI MOSFETs has been developed to address this problem by increasing the source/drain thickness, which is achieved by extending the source/drain regions deeper into the buried-oxide (Fig. 1) [6–11].

Subthreshold slope is a common parameter for characterization of the subthreshold operation and estimation of the transistor's off-state leakage current. Due to specific back-side of the ReS/D UTB SOI MOSFETs channel coupling to the vertical sidewall of the source and drain through the buried-oxide, the existing subthreshold slope analytical models for conventional SOI MOSFETs [12–15] are not applicable to ReS/D UTB SOI MOSFETs. SCEs are a common denomination of the subthreshold slope increase that is due to the loss of the electrostatic control of the gate over the potential barrier in the channel when the gate-length decreases. The subthreshold slope has to be small enough to ensure low leakage current and it is, therefore, desired to clarify the dependence of the subthreshold slope on the ReS/D UTB SOI MOSFET device parameters and the mechanism of its short-channel degradation with the channel-length shrinking.

Recently, we have studied SCEs in ReS/D UTB SOI MOSFETs by deriving analytical expressions for the two-dimensional (2-D) front-gate and back-gate surface potential distributions and for the threshold voltage [17]. Based on those analytical surface potential distributions, we derive a new analytical model for the subthreshold slope of the ReS/D UTB SOI MOSFETs, which is verified by comparing the model predictions with the simulation results obtained using numerical device simulator Medici [18]. This expression will then be used to analyze the dependence of subthreshold slope on various device parameters, such as channel length, gate material, gate-oxide thickness, silicon-body thickness, buried-oxide material, and thickness of the source/drain extensions in the buried-oxide.

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Nomenclature

C_{BOX}	buried-oxide capacitance
C_{GOX}	gate-oxide capacitance
C_{RSD}	recessed source/drain buried-oxide capacitance
$C_{Si,d}$	fully-depleted silicon-body capacitance
d_{BOX}	length of source/drain overlap over buried-oxide
k_{BOX}	buried-oxide dielectric constant
k_{GOX}	gate-oxide dielectric constant
k_{Si}	silicon-body dielectric constant
K_{BOX}	buried-oxide relative dielectric constant ($K_{BOX} = k_{BOX}/\varepsilon_0$)
K_{GOX}	gate-oxide relative dielectric constant ($K_{GOX} = k_{GOX}/\varepsilon_0$)
L	channel length
N_A	silicon-body doping concentration
N_{ASub}	substrate doping concentration
N_D	drain doping concentration
N_G	gate doping concentration
N_S	source doping concentration
S	subthreshold slope
V_{FB1}	front-gate flat-band voltage
V_{FB2}	source/drain-back-gate flat-band voltage
V_{FB3}	substrate-back-gate flat-band voltage
V_{th}	threshold voltage
Φ_M	gate work-function
Φ_{Si}	silicon-body work-function
$\Psi(x,y)$	electrostatic potential in the silicon-body
Ψ_b	difference between Fermi and intrinsic level
$\Psi_{s1}(y)$	front-gate surface potential at the gate-oxide-silicon-body interface [$\Psi_{s1}(y) \equiv \Psi(0,y)$]
$\Psi_{s1}(y_{min,s1})$	minimum front-gate surface potential
$\Psi_{s2}(y)$	back-gate surface potential at the silicon-body-buried-oxide interface [$\Psi_{s2}(y) \equiv \Psi(t_{Si},y)$]
$\Psi_{s2}(y_{min,s2})$	minimum back-gate surface potential
t_{RSD}	thickness of the source/drain extensions in the buried-oxide
t_{BOX}	buried-oxide thickness
t_{GOX}	gate-oxide thickness
t_{Si}	silicon-body thickness
V_{bi}	built-in potential
V_G	gate voltage
V_{DS}	drain–source voltage
$y_{min,s1}$	position of the front-gate surface potential minimum
$y_{min,s2}$	position of the back-gate surface potential minimum

2. ReS/D UTB SOI MOSFET modeling

ReS/D UTB SOI MOSFET's structure cross-section with the definition of geometrical characteristics and interface potentials is shown in Fig. 1. Using the parabolic potential approximation in the device body proposed in [16] we have developed a model for the potential distribution at the front-gate interface $\Psi_{s1}(y)$ and the back-gate interface $\Psi_{s2}(y)$ of the ReS/D UTB SOI MOSFETs in the subthreshold mode of operation [17]. The parabolic approximation of the electrostatic potential has been shown to give accurate prediction of the threshold voltage down to channel lengths in 20 nm range, while at the same time allowing a clear insight into the dependence of V_{th} on different physical quantities and device parameters, such as geometrical dimensions and material properties. The potential distribution along the channel at the front-gate interface $\Psi_{s1}(y)$ and the back-gate interface $\Psi_{s2}(y)$ of the ReS/D UTB SOI MOSFETs operating in depletion region, can be expressed with good accuracy, as follows from [17]:

$$\Psi_{si}(y) = A_{si}e^{\sqrt{\alpha_{si}}y} + B_{si}e^{-\sqrt{\alpha_{si}}y} + C_{si} \quad \text{for } i = 1,2, \tag{1}$$

where substitutions A_{si}, B_{si}, and C_{si} are

$$A_{si} = \frac{\beta_{si}(e^{\sqrt{\alpha_{si}}L} - 1) + \alpha_{si}[V_{bi}(e^{\sqrt{\alpha_{si}}L} - 1) + V_{DS}e^{\sqrt{\alpha_{si}}L}]}{\alpha_{si}(e^{2\sqrt{\alpha_{si}}L} - 1)}, \tag{2}$$

$$B_{si} = \frac{e^{\sqrt{\alpha_{si}}L}\{\beta_{si}(e^{\sqrt{\alpha_{si}}L} - 1) + \alpha_{si}[V_{bi}(1 - e^{\sqrt{\alpha_{si}}L}) + V_{DS}]\}}{\alpha_{si}(e^{2\sqrt{\alpha_{si}}L} - 1)}, \tag{3}$$

$$C_{si} = -\frac{\beta_{si}}{\alpha_{si}}. \tag{4}$$

L is the channel length (Fig. 2), V_{DS} is the drain–source voltage, $V_{bi} = (kT/q)\ln(N_{S-D}N_A/n_i^2)$ is the built-in potential (N_A is the silicon-body doping concentration, N_{S-D} is the source/drain doping concentration, and n_i is the intrinsic concentration). In the case of front-gate interface potential distribution $\Psi_{s1}(y)$, α_{s1} and β_{s1} are given:

$$\alpha_{s1} = 2\cdot\frac{1 + \frac{C_{GOX}}{C_{Si,d}} + \frac{C_{GOX}}{2C_{RSD}+C_{BOX}}}{t_{Si}^2\left(1 + \frac{2C_{Si,d}}{2C_{RSD}+C_{BOX}}\right)}, \tag{5}$$

$$\beta_{s1} = \frac{qN_A}{k_{Si}} - \frac{2(V_G - V_{FB1})\cdot\frac{C_{GOX}(C_{Si,d}+2C_{RSD}+C_{BOX})}{C_{Si,d}(2C_{RSD}+C_{BOX})} - (V_{DS} - 2V_{FB2})\cdot\frac{2C_{RSD}}{2C_{RSD}+C_{BOX}} - (V_{Sub} - V_{FB3})\cdot\frac{2C_{BOX}}{2C_{RSD}+C_{BOX}}}{t_{Si}^2\left(1 + \frac{2C_{Si,d}}{2C_{RSD}+C_{BOX}}\right)}, \tag{6}$$

where $C_{GOX} = k_{GOX}L/t_{GOX}$ is the gate-oxide capacitance per channel width (k_{GOX} is the gate-oxide dielectric constant, t_{GOX} is the gate-oxide thickness), $C_{Si,d} = k_{Si}L/t_{Si}$ is the fully-depleted silicon-body capacitance (k_{Si} is the silicon dielectric constant, t_{Si} is the silicon-body thickness), V_G is the gate voltage, $V_{FB1} = \Phi_M - \Phi_{Si}$ is the front-gate flat-band voltage, Φ_M is the gate work-function, and $\Phi_{Si} = \chi_{Si}/q + E_{G,Si}/2q + (kT/q)\ln(N_A/n_i)$ is the silicon-body work-function (χ_{Si} is the electron affinity, $E_{G,Si}$ is the bandgap). The buried-oxide region has been modeled using two capacitive couplings: (i) buried-oxide capacitance $C_{BOX} = k_{BOX}L/t_{BOX}$ (k_{BOX} is the buried-oxide dielectric constant, t_{BOX} is the buried-oxide thickness) that describes the coupling of the channel back-side to the substrate, which is assumed to be grounded; (ii) the recessed source/drain buried-oxide capacitance $C_{RSD} = k_{BOX}\ln(1 + L/2d_{BOX})/\theta$ (d_{BOX} is the length of source/drain overlap over buried-oxide) that describes coupling of the channel back-side to the vertical sidewall of the source and drain (Fig. 2). The recessed source/drain buried-oxide capacitance C_{RSD} has specific, two-dimensional properties and its analytical relation is given by an approximation of capacitive coupling between two perpendicular planes [17,19,20]. The angle $\theta = \pi/2 + \pi/2\cdot\text{sech}(t_{RSD}/d_{BOX})$ is the effective angle between the capacitor electrodes which varies between $\pi/2$ and π when $t_{RSD} \to 0$ that corresponds to the conventional UTB SOI MOSFET (t_{RSD} is the thickness of the source/drain extensions in the buried-oxide). For the channel lengths where $t_{RSD} < L/2$, the analytical relation is $C_{RSD} = k_{BOX}\ln(1 + t_{RSD}/d_{BOX})/\theta$. $V_{FB2} = (kT/q)\ln(N_{S-D}N_A/n_i^2)$ is the source/drain-back-gate flat-band voltage (N_{S-D} is the source/drain doping concentra-

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