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Sub-bandgap optical subthreshold current spectroscopy for extracting energy distribution of interface states in nitride-based charge trap flash memories

Kichan Jeon, Sunyeong Lee, Dong Myong Kim, Dae Hwan Kim *

School of Electrical Engineering, Kookmin University, 861-1, Jeongneung-dong, Seongbuk-gu, Seoul 136-702, Republic of Korea

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ABSTRACT

A sub-bandgap optical subthreshold current spectroscopy (OSCS) is proposed for extracting the energy distribution of interface trap density (D_{it}) in nitride-based charge trap flash (CTF) memory devices. It is based on the optical response of the subthreshold slope under sub-bandgap photonic excitation. By using the OSCS technique, we comparatively investigated the dominant energy range of the program/erase (P/E) cycling-induced D_{it} and observed that it is shallow in NROM-type operation and deep in NAND-type operation. Because no electrical pulse is required during extraction and the current is measured not from the substrate contact but from the drain contact, the OSCS technique is expected to be more useful for emerging nano-scale devices in comparison with the conventional charge pumping technique.

1. Introduction

Nitride-based charge-trap flash (CTF) memories have been recognized as one of promising next generation electrically erasable programmable read-only memories (EEPROMs). They have many advantages of simple fabrication process, small bit size, low voltage operation, multi-bit operation, suppressed drain-induced turn-on, and compatibility with scaled complementary metal–oxide-semiconductor (CMOS) technology [1,2]. However, the retention characteristic of CTF memories after program/erase (P/E) cycling is a crucial issue to improve through comprehensive characterization and practical modeling of relevant physical mechanisms. A large number of P/E cycling is well known to inevitably degrade the tunnel oxide, and the stress-induced leakage current (SILC) is known to result from increased interface traps and oxide traps. They cause critical reliability issues on the endurance, long-term retention, and disturbance of memory cells [3]. Furthermore, the energy distribution of traps in the tunnel oxide/Si substrate interface (N_{it} [cm^{-2}]) and traps in the bulk tunnel oxide (N_{OT} [cm^{-3}]) is closely related to the degradation mechanism induced during the P/E cycling in CTF memories. Therefore, accurate and efficient extraction of the distribution of energy-dependent interface traps (D_{it} [cm^{-2} eV^{-1}]) becomes significantly important as the thickness of the tunnel oxide is scaled down. This is because the charge loss is influenced by the trap-assisted tunneling as well as by the thermal emission or the Poole–Frenkel emission [4] as schematically shown in Fig. 1.

In conventional metal–oxide-semiconductor field-effect transistors (MOSFETs), the electrical charge pumping (*CP*) technique is most known to be useful for extracting N_{OT}, N_{it}, D_{it}, and the capture cross-section of interface traps [5–7]. However, it is hard to single out the pure charge pumping current (I_{CP}) in nano-scale MOSFETs with an ultra-thin gate oxide due to the incorporation of a large gate tunneling current into the pure I_{CP} [8,9].

Moreover, in order to make the quantity of pure I_{CP} component in nano-scale MOSFETs measurable, a high frequency pulse has been often applied by using an external pulse generator. Then, the I_{CP} under the measurement setup of a high frequency pulse can be greatly distorted by parasitic capacitances and resistances of metal pads, probe lines, and interconnect lines. Furthermore, an overshoot of the high frequency pulse caused by parasitic capacitances may increase the gate tunneling current during the conventional *CP* characterization. In addition, the conventional *CP* technique is hard to apply to nano-scale devices implemented on silicon-on-insulator (SOI) substrates [10,11], which is because the I_{CP} is measured via the substrate contact. It means that the electrical *CP* technique is not appropriate for emerging nano-scale devices, such as CTF memories, in that they should be characterized and optimized under various P/E stress conditions and innovative structures.

In this work, the *optical subthreshold current spectroscopy* is proposed as a simple and fast technique for extracting D_{it} in

* Corresponding author. Tel.: +82 2 910 4872; fax: +82 2 910 4449.
E-mail address: drlife@kookmin.ac.kr (D.H. Kim).

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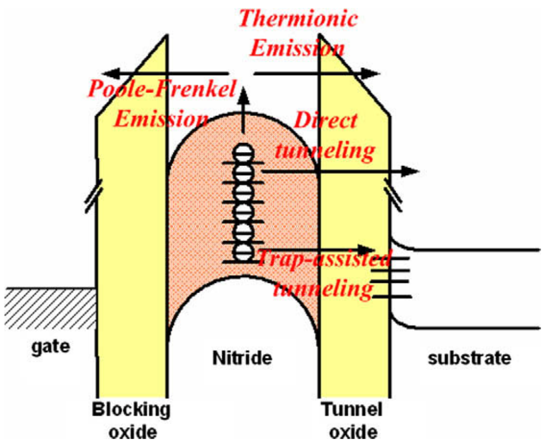

Fig. 1. Charge loss mechanisms in nitride-based CTF memories.

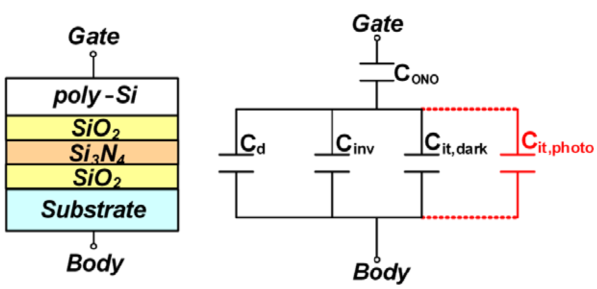

Fig. 2. Equivalent capacitive circuit model for CTF memory devices. The $C_{it,photo}$ is the capacitance component originated from the photo-excited carriers in the photo-responsive energy range of D_{it} only under optical illumination.

nitride-based CTF memory devices. It is based on the optical response of the subthreshold current under photon excitation with the photon energy (E_{ph}) smaller than Si bandgap energy ($E_{g,Si}$ = 1.1 eV). In addition, the proposed technique is applied to the comparative characterization of P/E cycling-induced D_{it} in NAND-type and NROM-type operated CTF memories. We expect that this technique is applicable to emerging nano-scale devices because there is no electrical pulse applied during the characterization and the current is measured directly from the drain contact, not from the substrate contact as is the case in the conventional *CP* technique.

2. Model of the sub-bandgap optical subthreshold current spectroscopy

In the proposed optical subthreshold current spectroscopy (OSCS) for extracting D_{it}, an optical source with a sub-bandgap photon energy (E_{ph} = 0.95 eV < $E_{g,Si}$ = 1.1 eV) is employed in order to optically pump trapped electrons only from N_{it}s to the Si conduction band ($E \geqslant E_C$) [12,13] while excluding the band-to-band electron–hole pair (EHP) generation in the Si substrate. Optical source can be changed to be smaller than the energy bandgap of the interfacial layers to be probed. An equivalent capacitance model under optical illumination is shown in Fig. 2 with C_{ono} as the equivalent capacitance of the top oxide/nitride/tunnel oxide (O/N/O) layers. C_d and C_{inv} as the depletion capacitance and the inversion layer capacitance, respectively. The $C_{it,dark}$ and $C_{it,photo}$ are the capacitance due to the interface charge modulation under dark and under optical illumination, respectively. Therefore, the $C_{it,photo}$ is originated from the photo-excited carriers in the photo-responsive energy range of D_{it} and activated only under optical illumination.

Schematic energy band diagrams of the CTF memory cell transistor under a sub-bandgap optical illumination are shown in Fig. 3. The photo-responsive energy range of the interface traps (ΔE) is modulated by both the surface potential (ψ_s) through the gate–source voltage ($V_{GS} = V_{FB} + \psi_{ONO} + \psi_s$) and the photon energy (E_{ph}). As shown in Figs. 3a and b, the photo-responsive range of E_{it} (interface trap energy level) is distributed as follows: $(E_C - E_{ph}) < E_{it} < E_{Fi}$ at a midgap condition ($V_{GS} = V_{midgap}$) and $(E_C - E_{ph}) < E_{it} < (E_{Fi} + q\phi_f)$ at a threshold condition ($V_{GS} = V_T$). Here, E_{Fi} and ϕ_f are the intrinsic Fermi-energy level (midgap) and the substrate doping (N_A)-dependent Fermi potential (=$kT/q \times \ln(N_A/n_i)$), respectively.

The subthreshold drain current (I_D) biased at $V_{GS} < V_T$ and the drain–source voltage (V_{DS}) can be written as [14,15]

$$I_D = I_{Do} \exp\left(\frac{V_{GS} - V_T}{\eta V_{th}}\right)\left\{1 - \exp\left(-\frac{V_{DS}}{V_{th}}\right)\right\}, \quad (1)$$

where the V_{th}(=kT/q) is the thermal voltage and the η is the ideality factor. Then, I_{Do} can be described by

$$I_{Do} = \mu_{eff} C_{ono}\left(\frac{W}{L}\right)(\eta - 1)V_{th}^2 = \mu_{eff} C_{ono}\left(\frac{W}{L}\right)\left(\frac{C_d + C_{it}}{C_{ono}}\right)V_{th}^2$$
$$\cong \mu_{eff} C_d\left(\frac{W}{L}\right)V_{th}^2, \quad (2)$$

$$\eta = 1 + \frac{C_d}{C_{ono}} + \frac{C_{it}}{C_{ono}}, \quad (3)$$

where the μ_{eff} is the effective channel carrier mobility and the W/L is the channel width-to-length ratio of the nitride-based CTF memory cell transistor. We also note that the depletion capacitance per unit area C_d (=ε_{Si}/X_d with a depletion layer thickness; $X_d = \sqrt{2\varepsilon_{Si}\psi_S/qN_A}$) depends on V_{GS} through the surface potential ψ_s at the Si/SiO_2 interface. The drain current without optical illumination ($I_{D,dark}$) can be re-described as

$$I_{D,dark} = I_{Do,dark} \times \exp\left[\frac{V_{GS} - V_{T,dark}}{\eta_{dark} V_{th}}\right] \quad \text{for } V_{DS} > 3V_{th}, \quad (4)$$

where η_{dark} is the ideality factor under dark condition. As a coupling factor of V_{GS} to the modulation of the channel conductivity, the ideality factor is written as

$$\eta_{dark}(V_{GS}) = 1 + \frac{C_d(V_{GS})}{C_{ono}} + \frac{C_{it,dark}(V_{GS})}{C_{ono}}. \quad (5)$$

Due to excess carriers generated by sub-bandgap photons through traps and interface states over the bandgap, the drain current ($I_{D,photo}$) under sub-bandgap photonic excitation can be modified into

$$I_{D,photo}(V_{GS}) = I_{Do,photo} \times \exp\left[\frac{V_{GS} - V_{T,photo}(V_{GS})}{\eta_{photo}(V_{GS}) \times V_{th}}\right] \quad \text{for } V_{DS} > 3V_{th}, \quad (6)$$

with the modified ideality factor (η_{photo})

$$\eta_{photo}(V_{GS}) = 1 + \frac{C_d(V_{GS})}{C_{ono}} + \frac{C_{it,dark}(V_{GS})}{C_{ono}} + \frac{C_{it,photo}(V_{GS})}{C_{ono}}, \quad (7)$$

where $V_{T,photo} = V_T - \Delta V_T$ and ΔV_T is the change of V_T due to the photovoltaic effect.

The V_{GS}-dependent (i.e., ψ_s-dependent) ideality factors (η_{photo} and η_{dark}) can be obtained from the subthreshold slope in the log(I_D) – V_{GS} curve in the subthreshold region and the η_{photo} has the information on the trap generated additional capacitance $C_{it,photo}$ under sub-bandgap photonic excitation. Here, all of C_d, $C_{it,dark}$ and $C_{it,photo}$ depend on V_{GS} through ψ_s. Because there is no band-to-band EHP generation in the substrate under sub-bandgap photonic excitation, it can be assumed that there is no change in C_d due to sub-bandgap photon. However, only $C_{it,photo}$ depends on the