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DC and RF characterization of AlGaN/GaN HEMTs with different gate recess depths

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This work compares AlGaN/GaN high-electron-mobility transistors (HEMT) with different gate recess depths. Small signal analysis showed that the best device performance was achieved at an appropriate recess depth primarily that was associated with maximized intrinsic transconductance and minimized source resistance. An $f_T \times L_g$ product of as high as 25.6 GHz-μm was obtained in a device with a gate recess depth of 10 nm. Further increasing the recess depth lowered the intrinsic transconductance and thereby worsened the performance. This effect was explained by the degradation of transport properties by the epitaxial damage that was itself caused by plasma-assisted dry etching processes.

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1. Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) are promising for RF power applications because of their high breakdown field and high saturation velocity. HEMTs have already been fabricated on SiC substrates with an f_T of 181 GHz, and an f_{MAX} of 186 GHz at a gate length of 30 nm [1], an output power density of 41.4 W/mm and a power-added efficiency (PAE) of 60% at 4 GHz [2]. In spite of these achievements, further improvement in device performance with a gate length of less than 0.2 μm has been primarily limited by a poor aspect ratio. The gate recess approach is a widely accepted method for overcoming this limitation [3,4]. Both intrinsic equivalent circuit and charge control models demonstrate elevated transconductance and performance improvement when the gate recess is used [5,6]. Additionally, owing to the difficulty of wet etching GaN and AlGaN compounds, plasma-assisted dry etching is generally used for fabricating recessed gates. The effect of the plasma-related process on gate leakage, breakdown voltage, surface trap density, and power performance has been reported elsewhere [7–10].

This work systematically investigates the impact of gate recess depth on DC and RF performance. An equivalent small signal model that includes intrinsic and parasitic components is utilized to understand the parameters that dominate the performance variation and to evaluate any potential limitation of the recessed-gate approach with the inductively coupled plasma dry etching.

2. Experimental

AlGaN/GaN heterostructure epitaxy materials were grown by metal organic chemical vapor deposition (MOCVD) on a 2-inch c-face sapphire substrate. They consisted of a 5 nm n^+-GaN (1×10^{19} cm^{-3}) layer, a 30 nm undoped $Al_{0.26}Ga_{0.74}N$ layer, and a 3 μm undoped GaN layer, in that order from the surface to the substrate. Fig. 1 plots the Hall results of the as-grown epitaxy sample and those with nominal etching recess depths of 5, 15, and 25 nm that were prepared by the inductively coupled plasma (ICP) dry etching. Electron mobility (μ_e) declined as the etching recess depth increased, while the sheet charge density (N_s) was maximized at an etching recess depth of 5 nm. The maximized sheet charge density obtained at the etching recess depth is due to cancellation of anti-parallel piezoelectric polarization between the n^+-GaN cap and the $Al_{0.26}Ga_{0.74}N$ top barrier layers, resulting in the increased piezoelectric charges at the interface of the $Al_{0.26}Ga_{0.74}N$ top barrier and the GaN buffer layers [11,12]. Because of the increase in the sheet charge density, the sheet resistance (R_{sh}), which is inversely proportional to the product of the mobility and the sheet charge density, reaches its lowest value of 410 ohm/sq. at the etching recess depth of 5 nm, suggesting that one of the parasitic resistances, which is associated with the device access region, can be minimized at this etching recess depth, enhancing high-frequency performance.

Device fabrication started with mesa definition, which was made by the ICP in a BCl_3/Cl_2-based plasma atmosphere, and was followed by the deposition of Ti/Al/Ni/Au source and drain ohmic metals. After rapid thermal annealing (RTA) at 850 °C for 35 s in

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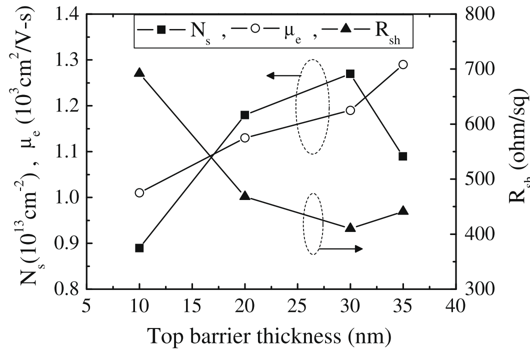

Fig. 1. Carrier density, mobility and sheet resistance as function of etching recess depth.

Table 1
Summary of important device characteristics of AlGaN/GaN HEMTs with gate recess depths of 0, 10, and 20 nm, respectively.

	0 nm gate recess	10 nm gate recess	20 nm gate recess	Note
I_{DSS} (mA/mm)	655.3	612.7	528.2	At V_{GS} = 0 V
$g_{m,peak}$ (mS/mm)	120.1	134.3	126.4	At V_{DS} = 10 V
V_{th} (V)	−6.2	−5.3	−4.3	At I_D = 1 mA/mm
R_{on} (ohm-mm)	5.5	7.5	8.7	At V_{DS} = 10 V
I_{on}/I_{off}	9.8E + 4	5.0E + 3	2.6E + 3	
SS (mV/dec)	182.3	263.8	436.0	
f_T (GHz)	7.6	12.8	9.6	
f_{MAX} (GHz)	23.6	46.0	37.8	

nitrogen ambient to form the ohmic contacts, the highly doped n$^+$-GaN cap was selectively removed by the ICP using the ohmic metals as hard masks. The gate recess was dry-etched and Ni/Au gate metals were subsequently deposited on a photolithographic gate pattern. Recessed Schottky gates were thereafter fabricated on the $Al_{0.26}Ga_{0.74}N$ top barrier layer after the gate metals on the photo resists were lifted off. The gate recess depths that were chosen in this work were 0, 10, and 20 nm. Finally, the probing pads of Ti/Au metals were made. TLM measurement indicated a contact resistance of ∼0.6 Ω-mm in all samples. The gate length (L_g) and width (W_g) were 2 and 50 × 2 μm, respectively, and the source-to-drain and gate-to-drain spacings were 6.0 and 2.0 μm, respectively. Fig. 2 schematically depicts the cross-sections of the three devices, which feature the ohmic contact area where the n$^+$-GaN cap layer is present under the ohmic metals for lowering the contact resistance, the device access area where the sheet resistance is minimized by removing the n$^+$-GaN cap layer, and the intrinsic device area where the recessed gate is fabricated. The effect of gate recess depth on DC and RF performance is evaluated.

3. Results and discussions

Table 1 lists important DC characteristics, which were obtained from the *I–V* and transfer curves of the three devices with different gate recess depths. The devices have a smaller drain saturation current (I_{DSS}) and a larger on resistance (R_{on}) when their gate recess depths are higher. This trend is primarily due to the added carrier depletion produced by surface electric field and the degraded carrier mobility, as suggested in Fig. 1. Moreover, the threshold voltage (V_{th}) increases with the recess depth because of the decreased Schottky barrier thickness and carrier density. With respect to the subthreshold drain characteristics, the subthreshold slope (SS) increases and the I_{on}/I_{off} ratio decreases as the gate recess depth increases. The I_{off} values obtained at high reverse gate biases dominate the subthreshold behavior, although the gate recess depth weakly affects the I_{on} value. Since dry etching easily produces plasma-induced surface traps and leakage paths [13], the devices that were exposed to the plasma ambient for longer tended to exhibit more serious degradation in their subthreshold behavior. Contrary to the subthreshold degradation caused by the dry etching of recessed gates, peak transconductance ($g_{m,peak}$) and frequency performance were highest in the device with a gate recess depth of 10 nm. Restated, a moderate gate recess promotes device performance but an excessive recess depth adversely affects performance. A similar trend has been found elsewhere [6]. An equivalent circuit model will be used later to extract all relevant small signal parameters to elucidate this phenomenon.

The Schottky gate behaviors and off-state drain leakages of the three devices with different gate recess depths were examined (Fig. 3a and b). Both gate and drain leakages increased with the recess depth. Setting 1 mA/mm drain current as the breakdown criterion yielded off-state breakdown voltages of 99, 88, and 70 V for the devices with 0, 10, and 20 nm gate recess depths, respectively (Fig. 3b). The turn-on voltage of the Schottky gates increased from 0.85 to 1.3 V as the recess depth increased, as shown in the inset in Fig. 3a, suggesting that the negatively charged chlorine ions that were introduced during the dry etching of the gate recess accumulated in the top barrier layer, causing upward bending of the conduction band edge [14]. The increase in barrier height increased the turn-on voltage. Furthermore, the accumulated chlorine ions and the epitaxy damage that was caused by the dry etching increased the trap state density of the Schottky barrier layer and thus enhanced the probability of trap-assisted tunneling [15]. The increase in the electric field by the increase in the gate recess depth produces an elevated leakage current, which degrades the breakdown voltage. We suggest either to optimize the dry etching recipe of the gate recess or to implement post-annealing for alleviating the impact of the plasma-induced degradation on the Schottky gate [10,16].

Microwave performance was measured using an HP8510 network analyzer. Current gain (h_{21}) and Mason's unilateral gain (U) were used to determine the cut-off frequency (f_T) and the maximum oscillation frequency (f_{MAX}), respectively. As mentioned

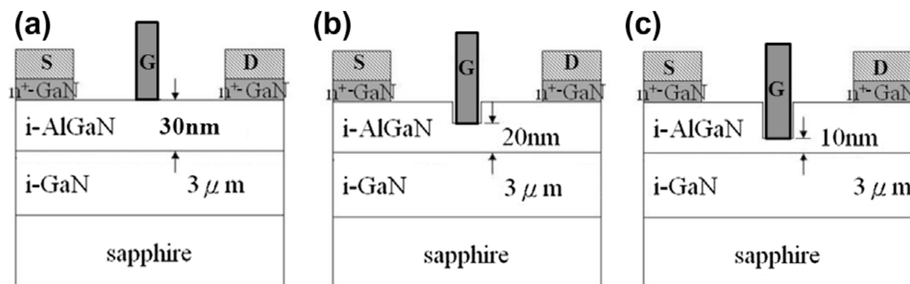

Fig. 2. Cross-sectional schematics of AlGaN/GaN HEMTs with gate recess depth of (a) 0, (b) 10, and (c) 20 nm, respectively.

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