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# Overview and future challenges of floating body RAM (FBRAM) technology for 32 nm technology node and beyond

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ABSTRACT

Floating body cell (FBC) is a one-transistor memory cell on SOI substrate aimed at high-density embedded memory on SOC. In order to verify this memory cell technology, a 128 Mb floating body RAM (FBRAM) with FBC has been designed and successfully developed. The memory cell design and the experimental results, including single-cell operation, are reviewed. Based on the experimental results, the scalability of FBC down to 32 nm technology node is also discussed.

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## 1. Introduction

Some kinds of capacitor-less DRAM cell have been proposed and developed [1–17]. Floating body cell (FBC) is a promising candidate in view of its simple structure and scalability. FBC and other embedded memories are compared in Table 1. We have named the RAM using floating body cell the floating body RAM (FBRAM). FBRAM has two operation modes: single-cell operation (1 Cell/Bit) and twin-cell operation (2 Cell/Bit). In the case of the single-cell operation, the memory cell size is $6F^2$, in which $F$ is the feature size. In the case of the twin-cell operation, the memory cell size is $12F^2$. The cell size of the single-cell operation is smaller than that of DRAM cell. In view of the single-cell operation, we think FBRAM can replace DRAM. The cell size of the twin-cell operation is also smaller than that of SRAM cell, and the access time is almost the same or the same order as that of SRAM. In view of the twin-cell operation, we think FBRAM can replace SRAM to a certain extent. The greatest advantage of FBRAM is its low cost because it dispenses with both the trench capacitor and the stack capacitor. On the contrary, for FBRAM for high-density embedded macro, one of the two key concerns is how to guarantee the memory cell characteristics such as the signal margin and the retention characteristics. The other key concern is scalability because of the reduction in the number of stored holes.

To verify the extendibility of FBC for embedded macros, a 128 Mb floating body RAM (FBRAM) has been designed and fabricated. It has been clarified that FBC has an adequate signal for the single-cell operation in the actual device operation condition. Based on the experimental results, the scalability of FBC down to 32 nm technology node has been investigated. The threshold voltage variation due to the random dopant fluctuation was estimated by the device simulation.

## 2. Memory cell design and fabrication of 128 Mb SOI DRAM

Fig. 1 shows a schematic view of the fabricated FBC structure. The memory cell consists of a one-transistor memory cell on SOI substrate with thin buried oxide. $P^-$ diffused layer on the substrate is used as a plate electrode, which can stabilize the body potential. Salicide process is introduced to reduce the parasitic resistance inside the array device, which is indispensable for high-speed write operation [8]. The write operation of FD FBC is shown in Fig. 2 [8]. Data "1" is written by creating holes by impact ionization and pushes up the body potential to a high level. Negative plate bias causes the created holes to accumulate at the back surface. On the other hand, data "0" is written by extracting holes from the body and pulls down the body potential to a low level. The stored signal can be distinguished using MOSFET current modulated by the body potential.

The memory cell layout and the design parameters are shown in Fig. 3 and Table 2, respectively. The unit cell area is $6.2F^2$ ($0.17\ \mu m^2$). The detail of the design of the array device has already

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**Table 1**
Comparison table of the embedded memories.

| | DRAM | eDRAM | FBRAM (1 Cell/Bit) | FBRAM (2 Cell/Bit) | SRAM |
|---|---|---|---|---|---|
| Cell size ($F^2$) | 6–8 | 12–20 | 6 | 12 | 80 |
| Process | CMOS + Capacitor | CMOS + Capacitor | CMOS | CMOS | CMOS |
| tRC (ns) | 20 | 5 | 20 | 3 | 1 |
| Advantage | High-density | High-performance | Low cost | Low cost | High-performance |
| Retention @ median (s) @85C | >10 | >1 | >0.1 | >0.1 | – |
| Issue to shrink | Capacitor transistor | Capacitor transistor | Transistor | Transistor | Transistor |
| Scalability limits | Storage capacitance | Storage capacitance | Hole density | Hole density | Signal stability |
| Basis of memory | Charge storage in capacitor | Charge storage in capacitor | Charge storage in floating body | charge storage in floating body | F–F |

been reported [8]. The thickness of SOI and BOX is 55 nm and 25 nm, respectively. To reduce the parasitic resistance, Co salicide is formed on the source, the drain and the gate. M1 (Cu wiring) was used both for the SL and the pad electrode for the BL contact. M2 (Cu wiring) was used for the BL. Fig. 4 shows a cross-sectional picture of the fabricated memory cell array in the BL direction. Function test with the single-cell operation using dummy cells [13] was carried out for the 16 Mb area under a simple write–read pattern. The results are shown in Fig. 5. A yield of 66.6% was obtained. There are some fail bits in good chips. But, we assume that these fail bits are fixed using the redundancy on the chip (64 fails are fixable in the 16 Mb area).

## 3. Memory cell characteristics

Different from the twin-cell operation, an adequate signal for the worst bit of 4.5$\sigma$ distribution must be guaranteed in order to realize single-cell operation. Both a large difference of the averaged read current between "1" and "0" cells' ($\Delta I_{cell} = I_{cell1} - I_{cell0}$) and a small standard deviation of read current ($\sigma_{I_{cell0}}$ *and* $\sigma_{I_{cell1}}$) are indispensable for getting superior chip yield. Here we have introduced an index of the signal sense margin (SSM), which predicts the memory chip yield. That is defined as

$$SSM = \Delta I_{cell} - \alpha(\sigma_{I_{cell0}} + \sigma_{I_{cell1}}) \quad (1)$$

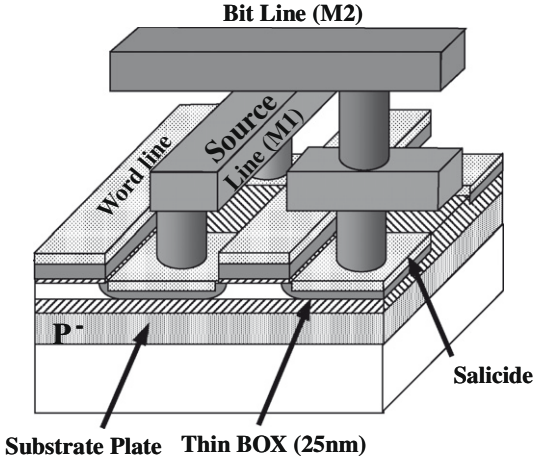


**Fig. 1.** Schematic view of FBC structure.

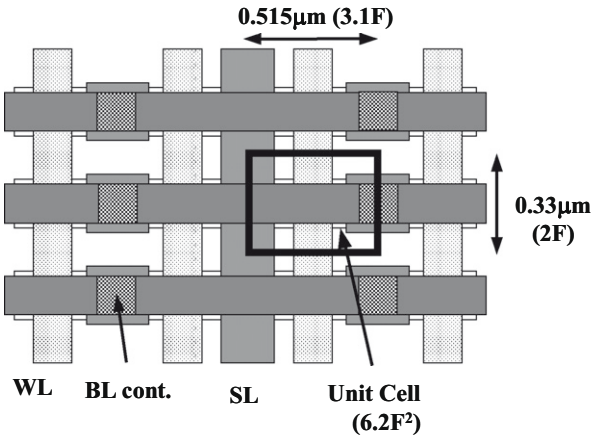


**Fig. 3.** Layout of a 128 Mb FBC array.

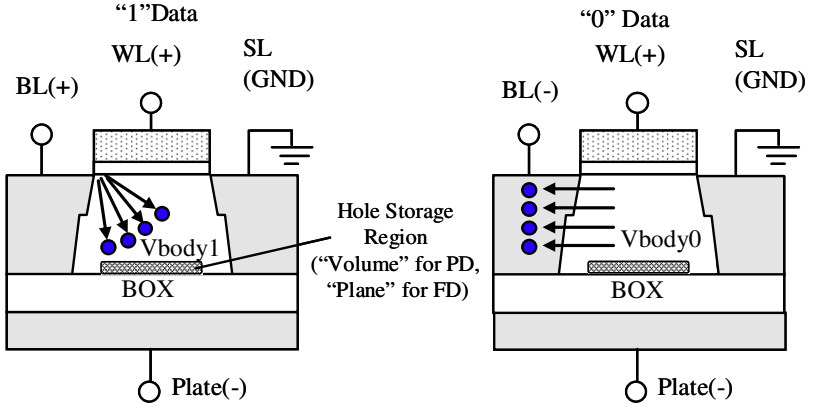


**Fig. 2.** Write operation of FD FBC.

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