Solid-State Electronics 53 (2009) 741-745

Contents lists available at ScienceDirect

# Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

# New floating-body effect in partially depleted SOI pMOSFET due to direct-tunneling current in the partial n+ poly gate

Georges Guegan<sup>a,\*</sup>, R. Gwoziecki<sup>a</sup>, P. Touret<sup>a</sup>, C. Raynaud<sup>a</sup>, J. Pretet<sup>b</sup>, O. Gonnard<sup>b</sup>, G. Gouget<sup>b</sup>, S. Deleonibus<sup>a</sup>

<sup>a</sup> CEA-LETI Minatec, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France <sup>b</sup> STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France

## ARTICLE INFO

Article history: Received 13 November 2008 Accepted 3 February 2009 Available online 21 April 2009

The review of this paper was arranged by Prof. P. Ashburn

Keywords: Silicon-On-Insulator (SOI) pMOSFET Direct-tunneling mechanism Body potential

#### ABSTRACT

A detailed analysis of the body potential impact on the performance enhancement of Body Contacted (BC) pMOSFET when the body is not grounded, is reported in this paper. Investigations on BC pMOSFET with a floating-body configuration reveal that this new floating-body effect leads to pMOSFET drive capability increase with higher transconductance, lower subthreshold slope, no off-state leakage current degradation and no kink effect. The body potential is mainly controlled by the electron tunneling from the conduction band (ECB) between the partial n+ poly-gate and the n type silicon substrate through the 1.6 nm thin gate oxide. Static characterizations of various layouts and geometries demonstrate that narrow pMOSFET and H-gate design provides the highest lon gain due to higher body potential. Furthermore, it has been found that the largest n+ poly-gate area results in the fastest switch-on drain current transients.

© 2009 Elsevier Ltd. All rights reserved.

#### 1. Introduction

The Silicon-On-Insulator (SOI) technology is very attractive in terms of high speed, low power dissipation, latch-up and soft-error immunities, co integration of digital and analog/RF circuits [1,2]. However, Partially Depleted (PD) SOI Metal-Oxide-Semiconductor-Field-Effect Transistors (MOSFETs) exhibit specific characteristics associated with either floating body (kink effect, transient bipolar effect, historic-dependent delay) or self-heating effects. With gate oxide scaling, the floating-body potential of PD SOI MOSFETs is not only controlled by electron-hole generation-recombination and impact-ionization mechanisms, but also by tunneling current. The Gate-Induced Floating-Body Effect (GIFBE) which has been observed in both PD SOI MOSFETs [3] and fully depleted transistors [4], leads to a second peak in transconductance of devices designed with 3-terminal without a tied body. The predominant components which flow between the gate and the channel have been investigated extensively for 3-terminal devices [5]. Few studies have focused on Body Contacted (BC) devices with floating-body configuration, i.e. the body potential is not controlled by the body contact [6,7]. Therefore, the purpose of this paper is to study statically and dynamically the BC MOSFET characteristics processed with thin gate oxide and various geometries with either T-gate or H-gate designs when the body contact is not grounded.

#### 2. Device structure

PD SOI MOSFETs used in this study were fabricated on SOITEC standard 300 mm Unibond<sup>®</sup> wafers with an advanced CMOS technology integration, featuring 1.6 nm physical gate oxide, 70 nm silicon film and 145 nm buried oxide. The fabrication was completed with a conventional back-end process including six copper metal levels and low k dielectrics. The power supply voltage is one volt (1 V). These SOI MOSFETs were designed with various layouts: 3terminals for no body tied devices, or BC devices with either T-gate design and one body contact on the side or H-gate layout with a body contact on each side, thus two contacts (Fig. 1). These body contacts may be grounded or left floating during device operation. The lateral poly-gate of BC pMOSFETs is partially covered by n+ implant to form the extra body terminal (Fig. 2). Therefore, the body contact of pMOSFET which is covered by n+ implant is defined by the following stack: n+ poly-gate, thin gate oxide and n type silicon film. The channel lengths and widths which are in the range 0.1-10 µm, allow to investigate the dimensional aspects of these new floating-body effects due to various ratios between n+/p+ poly-gate areas.





<sup>\*</sup> Corresponding author. Tel.: +33 4 38 78 48 10; fax: +33 4 38 78 94 56. *E-mail address:* georges.guegan@cea.fr (G. Guegan).

<sup>0038-1101/\$ -</sup> see front matter @ 2009 Elsevier Ltd. All rights reserved. doi:10.1016/j.sse.2009.02.011



**Fig. 1.** Top view layouts of 3-terminal (left) and H-gate PD SOI pMOSFETs with two body contacts (right).



**Fig. 2.** Cross-sectional view taken from line A–A of Fig. 1, illustrating H-gate PD SOI pMOSFETs with p+ poly-gate, partial n+ poly-gate and n type substrate.

## 3. Electrical results

Figs. 3 and 4 show Id–Vg, Ig–Vg and Ib–Vg characteristics of, respectively, BC pMOSFET and nMOSFET designed with a T-gate for the body contact. The source voltage and the body voltage are connected to ground. The body current characteristics of pMOSFET and nMOSFET are different: contrary to the nMOSFET behaviour, the body current of pMOSFET does not depend on drain voltage and is highly gate voltage dependent. In addition, the global behaviours of pMOSFET gate and body currents are similar while Ib–Vg



**Fig. 3.** Id–Vg, Ib–Vg and Ig–Vg at Vds = -100 mV and -1 V characteristics of pMOSFET whose body is grounded (*W*/*L* = 2.5  $\mu$ m/0.11  $\mu$ m).



**Fig. 4.** Id–Vg, Ib–Vg and Ig–Vg at Vds = 100 mV and 1 V characteristics of nMOSFET whose body is grounded (W/L = 2.5  $\mu$ m/ 0.11  $\mu$ m).

of nMOSFET is strongly drain voltage dependent and conventionally controlled by impact-ionization mechanism at high drain voltage. Therefore, static and transient dynamic measurements have been performed to clarify the behaviour of BC pMOSFET with either body tied or floating-body configuration.

# 3.1. Static characteristics

Fig. 5 shows typical output characteristics for 3-terminal and Hgate (two body contacts) either with a grounded body or with a floating-body configuration. If the body contact of BC pMOSFET is not connected, we observe a gain on Ion. Furthermore, the drive capability increase of the devices leads to a higher drain current in both linear and saturation regime than in a 3-terminal device with no kink effect. A weak inversion characteristic comparison (Fig. 6) shows a lower subthreshold slope for both low and high drain voltages due to a lower depletion capacitance variation with a floating-body configuration. Therefore, the off-state leakage current of BC devices with floating configuration is one decade lower than on the 3-terminal device loff which is degraded by the kink effect. A second peak of transconductance due to GIFBE is observed with the 3-terminal device due to both direct-tunneling currents between the channel and the p+ polysilicon gate and a sudden change of the body potential and the threshold voltage (Fig. 7). In contrast to the 3-terminal device, the body voltage of BC pMOS-



**Fig. 5.** Id–Vd comparison of H-gate with either body grounded or floating-body configuration and 3-terminal pMOSFET with Vg from 0 to -1 V by 0.2 V steps (*W*/  $L = 5 \mu m/0.11 \mu m$ ).

Download English Version:

https://daneshyari.com/en/article/747466

Download Persian Version:

https://daneshyari.com/article/747466

Daneshyari.com