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250 °C operation normally-off GaN MOSFETs

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Abstract

We tried normally-off operation GaN metal–oxide–semiconductor field effect transistors (MOSFETs). n+ Contact layers as a source and drain region were fabricated using a Si ion implantation technique with the activation annealing at 1300 °C for 30 s in Ar ambient. The ohmic contact and sheet resistance of n+ contact layer were 1.1×10^{-7} Ω cm^2 and 53 Ω/sq, respectively. As a result, we achieved a normally-off operation GaN MOSFETs and moreover high temperature operation of 250 °C for the first time. Threshold voltage (V_{th}) was +3 V. Drain current (I_d) was over 100 mA/mm at gate voltage (V_g) of 10 V and drain-to-source voltage (V_{ds}) of 10 V. Maximum field effect mobility (μ_{FE}) was 210 cm^2/V s at $V_{ds} = 0.1$ V.

Keywords: GaN; Power devices; Normally-off; High temperature operation; Enhancement mode

1. Introduction

The power transistors have been used for high power and high temperature devices, such as car electronics, home appliance, and so on. These devices are required to be more large power and lower on-state resistance under high temperature conditions. To date, Si based insulated gate bipolar transistors (IGBTs) have been used for high power devices. However, the device performance would be degraded under high temperature above 150 °C.

SiC based MOSFETs has been studied by many researchers. Mitsubishi Electric reported 3.7 kW/400 V motor operation using inverter with SiC MOSFETs [1]. However, the reliability has been insufficient, and its high temperature operation has not yet been realized.

The GaN has good excellent properties, such as high critical electric field and high saturation mobility compared with those of SiC and Si. Therefore, GaN power devices will be also stable compare to Si power devices under high temperature conditions.

AlGaN/GaN heterostructure field effect transistors (HFETs) have been recently studying, since a large electron density is easy to be obtained due to two dimensional electron gas (2DEG) generated by a piezo effect at the AlGaN/GaN interface.

We demonstrated inverter and converter circuits using AlGaN/GaN HFETs [2]. However, the threshold voltage (V_{th}) of the HFETs was negative, that is, the operation was normally-on mode. Therefore, the drive circuits for control of gate voltage are necessary.

On the other hand, the metal–oxide–semiconductor (MOS) field effect transistors (MOSFETs) have good points of the normally-off operation and lower gate leakage. Consequently, the GaN based n-channel MOSFETs can be a good candidate of power devices. Recently, several researchers reported the operation of MOSFETs [3–7]. Chow et al. reported 150 °C operation of GaN MOSFETs [4]. However, there is no report higher temperature operation above 150 °C.

SiO_2 is a good candidate as a gate oxide because of high critical electric field, robust at high temperature, large

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bandgap, and so on. Therefore, the inversion electrons could be easily confined at the interface between an oxide and a semiconductor.

However, to realize the operation of GaN MOSFETs, n+ contact layer with low ohmic contacts and the SiO_2/GaN interface with low interface characteristics will be necessary. It found that the interface states were reduced by annealing after SiO_2 deposition on GaN. We previously reported that the interface state density of SiO_2/n-GaN MOS capacitor was less than $1\times10^{11}\,cm^{-2}\,eV^{-1}$ at E_c – 0.4 eV from Terman method by annealing the SiO_2/n-GaN [8].

In this work, we have fabricated the GaN MOSFETs for high temperature at 250 °C operation. The ohmic contact resistance and sheet resistance of n+ contact layer were $1.1\times10^{-7}\,\Omega\,cm^2$ and 53 Ω/sq. by Si ion implantation with an activation annealing at 1300 °C for 30 min in Ar ambient. Finally, we have achieved 250 °C operation GaN MOSFETs with threshold voltage (V_{th}) of +3 V.

2. Experiment procedure

We have studied the activation annealing for forming the n+ contact layer. The Si ion as an n-type dopant was selected for conventional material. The screen oxide of 20-nm-thick SiO_2 was deposited on a p-GaN surface due to suppress the damage of implantation and adjusts depth profile of Si ions. Then, Si ion was implanted in p-GaN as following doses and energies: (1) $3\times10^{15}\,cm^{-2}$ and 190 keV, (2) $1\times10^{15}\,cm^{-2}$ and 120 keV, (3) $8\times10^{14}\,cm^{-3}$ and 60 keV, and (4) $4\times10^{14}\,cm^{-2}$ and 30 keV. The implanted depth was designed to be 300 nm by Lindhard, Scharff and Schiøtt (LSS) theory. Once removing the SiO_2 screen oxide, the SiO_2 as a capping layer was deposited on the GaN surface again. The rapid thermal annealing (RTA) was used for an activation annealing because Si atoms cannot diffused in the p-GaN layer. The sheet resistance was checked by Van der Pauw.

Then, we have fabricated the GaN MOSFET. Fig. 1 shows a schematic drawing of GaN MOSFETs. At first, the p-GaN ([Mg]=$1\times10^{17}\,cm^{-3}$–$5\times10^{17}\,cm^{-3}$) was epitaxially grown on a sapphire (0001) substrate. Then, n+ contact layer was formed by a Si ion implantation. An activation annealing was performed at 1300 °C for 30 s in Ar ambient by RTA. Next, 60-nm-thick SiO_2 as a gate oxide was deposited on a GaN surface. The SiO_2/GaN was annealed at 900 °C for 30 min in N_2 ambient for reducing the interface states [8]. After while, the Ti (25 nm) and Al (300 nm) as a source and drain electrode were evaporated on n+ contact layer by using sputter deposition equipments. After electrode annealing at 650 °C for 5 min in N_2, the ohmic contact resistance and sheet resistance were $1.1\times10^{-7}\,\Omega\,cm^2$ and 53 Ω/sq by TLM measurements. Then, Ti (25 nm) and Au (200 nm) as a gate electrode were evaporated on the SiO_2 layer using sputter deposition equipments.

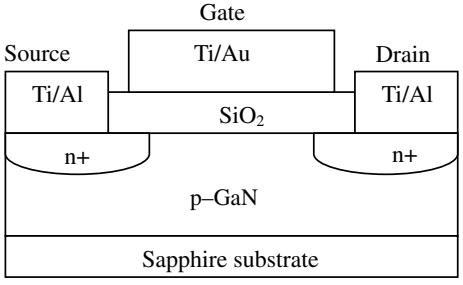

Fig. 1. Schematic of SiO_2/GaN MOSFETs.

3. Result and discussion

3.1. Activation of n+ contact layer

Figs. 2 and 3 show a sheet resistance of a Si implanted GaN. The sheet resistance was decreased 125 Ω/sq. as increasing temperature for 10 s as shown in Fig. 2. In addition, the sheet resistance was decreased up to 26 Ω/sq. as increasing time at 1300 °C as shown in Fig. 3. This means

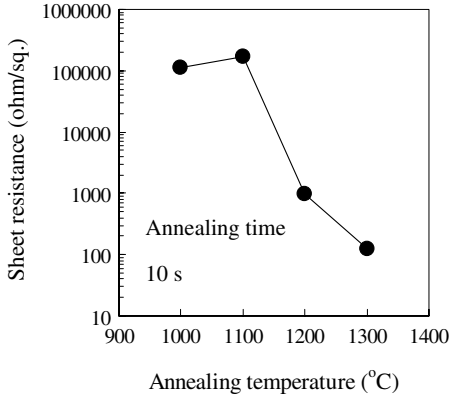

Fig. 2. Results of activation annealing of Si implanted GaN by RTA. Sheet resistance as a function of annealing temperature for 10 s in Ar ambient. The sheet resistance was estimated by Van der Pauw.

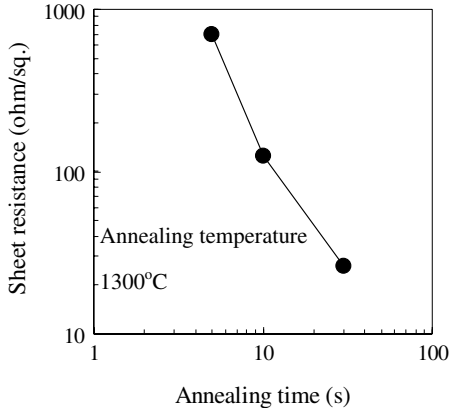

Fig. 3. Results of activation annealing of Si implanted GaN by RTA. Sheet resistance as a function of annealing time at 1300 °C in Ar ambient. The sheet resistance was estimated by Van der Pauw.