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Low-temperature nickel-induced nano-crystallization of silicon on PET by MIC, hydrogenation and mechanical stress

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Abstract

The effects of RF-Plasma hydrogenation and applied mechanical strain on the crystallization of silicon layers deposited on plastic substrates have been investigated where the maximum temperature remained below 170 °C for the entire process. The structural properties of the samples have been studied by optical, scanning-electron and transmission-electron microscopy where the nano-crystallinity of the silicon layers has been confirmed. The maximum average diameter of the silicon grains was 4.5 nm and occurred for an applied tensile strain of 4%. In addition, a thin-film transistor on a plastic substrate has been fabricated and found to possess an electron mobility of 2.4 cm^2/V s.
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1. Introduction

The performance of semiconductor devices generally improves with the level of crystallinity in the active layer; single crystals are superior to polycrystalline materials which are in turn superior to amorphous layers. When amorphous and polycrystalline materials are deposited on silicon substrates, the degree of crystallinity can be readily improved by high-temperature annealing. However, in applications requiring low-cost, flexible substrates such as glass or plastic, low processing temperatures must be maintained in order to avoid thermal degradation of the substrate and polycrystalline silicon becomes the material of choice. Two important applications of polycrystalline silicon are solar cells [1] and thin-film transistor (TFT) drivers in liquid-crystal displays [2]. In these cases, low cost substrates such as glass or Kapton are usually coated by an amorphous silicon layer and crystallization is achieved by means of a subsequent annealing step [3,4].

Several techniques are used for the crystallization of amorphous silicon including solid-phase crystallization (SPC), excimer-laser annealing (ELA) and metal-induced crystallization (MIC). One major limitation of the SPC method is that it requires relatively high temperatures and long processing times, conditions incompatible to many low-cost substrates [5–7]. Excimer laser annealing is a low temperature approach that is most frequently used at present, but it requires expensive apparatus to implement. On the other hand, MIC [8] is a promising technique which allows crystallization of the amorphous silicon layer at temperatures conducive to the use of low-cost glass and plastic substrates. In addition, metal-induced lateral crystallization (MILC), stress-assisted reorganization [9], hydrogenation [10] and several other techniques have been

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widely studied and characterized during the past two decades [11–13].

Recently, we have reported the reduction of the annealing temperature for the crystallization of silicon and germanium films by the application of an external mechanical stress in conjunction with the MIC method [14–18]. In these previous works, we have been able to demonstrate the crystallization of germanium-on-plastic at a maximum processing temperature of 130 °C; the crystallization of silicon-on-glass at a temperature of 310 °C; and the partial crystallization of $Si_{0.35}Ge_{0.65}$-on-plastic at a temperature of 180 °C. In this paper, we report for the first time the combined use of MIC, RF-plasma hydrogenation and the application of a mechanical stress for the crystallization of amorphous silicon layers on plastic substrates where the temperature during all of the processing steps remained below 170 °C. The nano-crystalline silicon materials were then used to fabricate a thin-film transistor.

2. Experimental setup

The flexible polyethylene terephthalate (PET) substrates were rinsed in dichloromethane and subsequently cleaned using RCA #1 solution ($H_2O_2/H_2O/NH_3$ 1:5:1) for 12 min. This was followed by a rinse in de-ionized water and the surface blown dry with nitrogen gas. The substrate was then placed under vacuum at a base pressure of 3×10^{-6} Torr and maintained at 120 °C during the electron-beam deposition of the silicon and metal layers. A tri-layer Si/Ni/Si structure was deposited with layer thicknesses of 500, 10 and 400 Å, respectively. Thickness of various layers was in situ monitored using an Inficon quartz crystal-microbalance. The nickel-silicide layer provides the seeds required to initiate the crystallization of silicon [19]. The thickness of the metal layer was set to about 1% of the total layer thickness in order to minimize the adverse effects of metal contamination in accordance with previous experience where Ni was successfully used to facilitate the low-temperature crystallization of silicon. The application of the mechanical stress is achieved by bending the sample inward or outward, depending on the type of the stress, whether compressive or tensile (see Fig. 1). The sample holder during the bending is made of stainless foils and the samples are tightened from their ends. Low temperature ovens are used to treat the samples during this long thermo-mechanical treatment step.

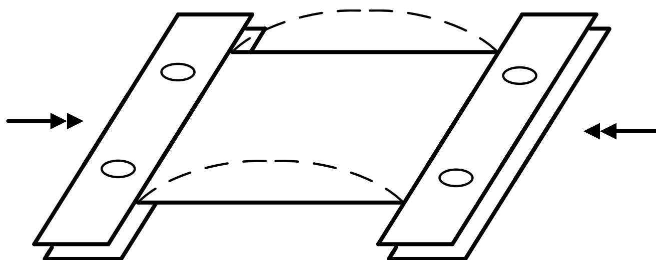

Fig. 1. Schematic setup for the bending of the sample. Sample is tightened from both sides to apply a proper compressive or tensile stress.

Fig. 2 presents a schematic diagram of the steps involved in the preparation of the specimens from the as-deposited Si/Ni/Si tri-layer (Fig. 2a) to the fabrication of a thin-film transistor (Fig. 2e). After deposition of the silicon and nickel layers the samples were placed in a UNAXIS-790 RF-PECVD system where they were subjected to a hydrogenation-anneal treatment (Fig. 2b). First the samples are exposed to RF-hydrogen plasma at a power of 250 W, a pressure of 200 mTorr, a substrate temperature of 120 °C, and for duration of 20 min. Plasma powers greater than 300 W were observed to partially etch the deposited Si layer and damage the PET substrate. A plasma power of 250 W was the maximum value that did not lead to etching of the substrate or the silicon layer for the durations and temperatures involved. It was observed that hydrogenation

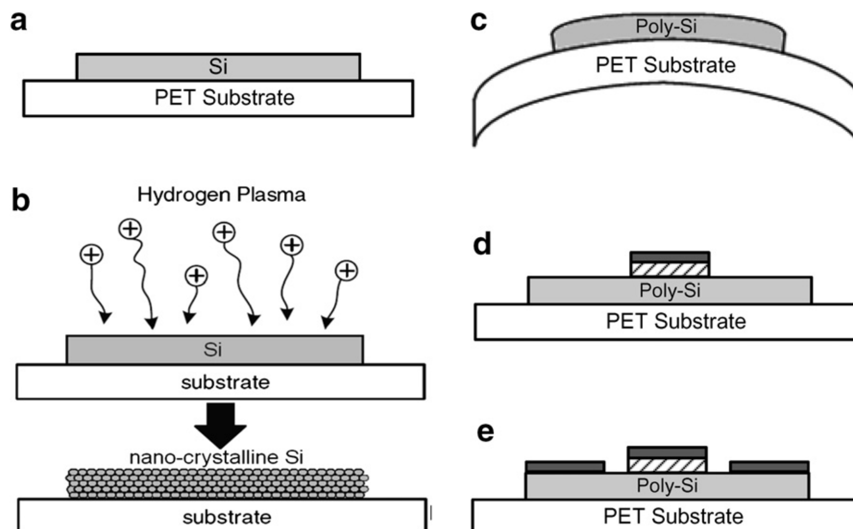

Fig. 2. A schematic view of the steps involved in the low-temperature crystallization of silicon and the fabrication of TFTs.

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