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Advanced memory concepts for DRAM and nonvolatile memories

Fumio Horiguchi *

Department of Computational Science and Engineering, Toyo University, 2100 Kujirai, Kawagoe, Saitama 350-8585, Japan

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Abstract

This paper describes the advanced DRAM and nonvolatile memory concepts, current status and challenges. Leading edge DRAM and nonvolatile memories are encountering scaling limitations such as transistor performance degradation and Vth variation. In order to overcome these constraints, three-dimensional approach is being adopted in many devices.

Keywords: DRAM; Nonvolatile; Three-dimensional; MRAM; Flash; Multi-layered

1. Introduction

As device scaling advances, memory cell integration encounters difficulties because of degraded transistor performance and degraded fine patterning. All these constraints spur interest in the three-dimensional structure approach to memory device applications. For the DRAM application, array transistor can be adopted such as the fin-type double gate or surrounding gate transistor structures. For the flash memory and FeRAM applications, series connection of memory cells is the key approach for a low-cost configuration. For the newly developed MRAM application, cross-point and multi-layered approaches will be important solutions.

2. Advanced DRAM technologies

As the DRAM cell size shrinks to sub-100 nm, it becomes critically important to realize sufficient on-current of the array transistor because of the limited channel width and the degraded electron mobility due to increased channel doping. Moreover, the conventional MOSFET scaling techniques should not be applied to the array transistor, because the gate oxide thickness should not be shrunk in view of the requirement of extreme low off-current for the data retention, which restricts the threshold voltage to around 1 V without extra channel doping. In view of these considerations, a different structural approach for array FET of DRAM is indispensable. Also, a new approach is required which increases storage capacitance within a limited capacitor area.

3. TIS/Fin/SGT DRAM

In order to overcome the array FET constraints, trench isolated transistor using sidewall gates (TIS) or fin-array-FET approach can be adopted to improve the transistor performance as in the case of SOI transistors [1–4]. Fig. 1 shows a bird's eye view of TIS-Array FET. TIS gate structure, which consists of top gate and side-wall gate enables high on-current and low off-current simultaneously because of the double gate structure and high gate controllability. Fig. 2 shows the T_{fin} dependency of the minimum L_g. The thinner T_{fin} is expected to result in a dramatic reduction of off-current, which is very suitable for array transistors.

A more advanced array transistor approach using surrounding gate transistor (SGT) will be adopted [5,6].

* Tel.: +81 492391548; fax: +81 492315026.
E-mail address: horiguti@eng.toyo.ac.jp

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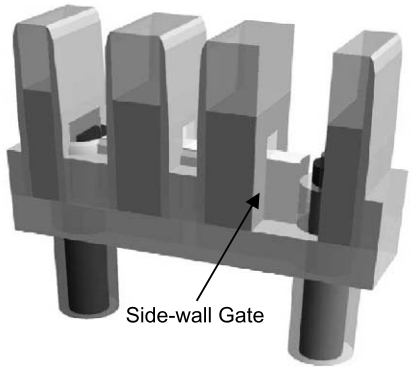

Fig. 1. TIS/fin array FET DRAM.

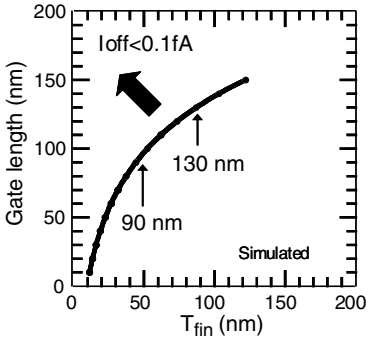

Fig. 2. Minimum gate length versus fin thickness.

SGT has great advantages, namely, high drivability and compact area which are suitable for DRAM array device.

The other prerequisite for enhancing the signal to noise ratio is to increase the capacitor dielectric constant. As scaling advances, the area available for capacitor decreases. Therefore, capacitance enhancement technologies such as hemispherical silicon grains and Al_2O_3 ALD high k dielectric are promising candidate [7].

DRAM scaling will continue to integrate many advanced technologies in view of the huge size of the DRAM market.

4. Floating body cell

The difficulties of DRAM integrations are mainly attributable to the necessity of constant capacitance when the cell size is shrunk. For this reason, the integration of capacitor is very complicated as a trench or a stacked capacitor is required. Floating body cell (FBC) is the new concept of capacitor-less DRAM. Fig. 3 shows the principle of FBC which involves storage of the signal charge in the body of cell transistor. Because the cell is composed of one transistor, FBC has simple and compact structure. In this case, back gate is used for the charge accumulation in the body [8–10]. This structure is the modified double gate configuration. Fig. 4 shows the TEM cross-section of fully depleted FBC, having thin SOI and BOX layers. FBC is suitable for high performance eDRAM applications.

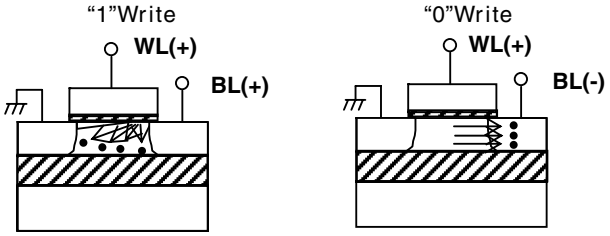

Fig. 3. Structure and advantage of FBC.

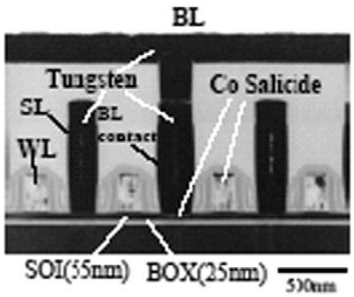

Fig. 4. Cross-sectional TEM of FBC.

5. NAND flash memory

NAND flash memory is used for file memories, e.g. in data storage for digital still camera and for cellular phones. The market for NAND flash memory is growing more rapidly than that for NOR flash memory, which is used for program memory in cellular phones. Fig. 5 shows the NAND/NOR flash memory market growth. NAND flash market is expected to increase significantly within a couple of years. This rapid increase is due to the widespread use of flash memory cards, USB memories and MP3 audio.

NAND flash memory scaling focuses on achieving a sufficient coupling ratio between control gate and floating gate. A conventional cell has two-layer floating gate as shown in Fig. 6. In order to shrink cell size, novel self-aligned shallow trench isolation cell was introduced from 90 nm technology onward. This cell is composed of floating gate self-aligned to active area. The coupling ratio is obtained by using top and sidewall of floating gate, and the interference between floating gates is effectively

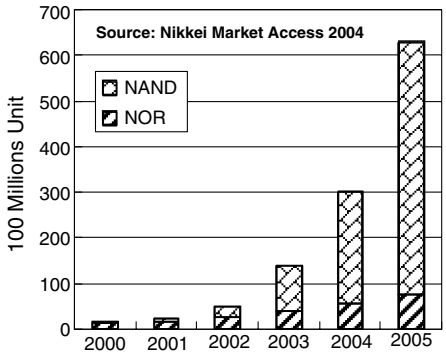

Fig. 5. NAND/NOR flash memory market counted as 16 Mbit capacity unit.