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Letter

Temperature control for the gate workfunction engineering of TiC film by atomic layer deposition

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ABSTRACT

The effects of the deposition temperature on titanium carbide film formed by atomic layer deposition are investigated for gate workfunction (WF) engineering. As the deposition temperature increases from 250 °C to 500 °C, the WF of the TiC decreases from 5.24 eV to 4.45 eV. This WF dependency on the deposition temperature is mainly attributed to the average WF of each orientation of the sub-planes of the TiC film. An investigation of a tunable WF is conducted through Auger electron spectroscopy, transmission electron microscopy, and X-ray diffraction.

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1. Introduction

With the aggressive scaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) to achieve high performance and high-density integration, a high-*k* and metal gate (HKMG) configuration has replaced the conventional SiO_2 and poly-crystalline silicon (poly-Si) stacks in memory as well as logic applications [1]. In HKMG technology, the workfunction (WF) of a gate metal is the main parameter used to control the threshold voltage (V_T) of MOSFETs [2]. Thus, studies of the WF engineering of metal films by changing the process variables during the metal deposition step and incorporating other elements into deposited metal have received a great deal of attention [3–6]. Among them, a number of TiC films reported thus far have shown good inherent properties as a gate electrode, such as high thermal stability (melting point of 3067 °C), low electrical resistivity (~68 μΩ cm), and high step coverage when they are deposited by atomic layer deposition (ALD) [7]. However, typically these reports focus not on the applicability to the MOSFET process but on the growth mechanism of TiC and fundamental characterizations of this material [7–9]. It is timely to investigate TiC film for the implementation to MOSFETs for improved practical use of this type of film.

Herein, the WF tunability of TiC film samples with various deposition temperatures is investigated in an effort to utilize TiC film as a gate metal in a MOSFET. Numerous investigations of gate stacks consisting of a material with a high dielectric constant (high-*k*) have been carried out recently with state-of-the-art CMOS technology. However, silicon dioxide (SiO_2) is deliberately used as a gate dielectric in the present study in order to focus on WF changes of the TiC film without parasitic effects such as distortion of the WF stemming from the interfacial dipole effect between the high-*k* material and the metal film [10]. In this report, we observe the WF tunability of TiC films according to the deposition temperature and analyze the origin of such tunability with Auger electron spectroscopy (AES), transmission electron microscopy (TEM), and mainly X-ray diffraction (XRD).

2. Experimental

In the experiment, TiC films were formed by a super-cycling method which involved a titanium (Ti) sub-cycle and a carbon (C) sub-cycle in an ALD system. Titanium tetrachloride ($TiCl_4$) and trimethylaluminum (TMA; $(CH_3)_3Al$) were used as the precursors for Ti and C, respectively. In contrast to the conventional ALD process, which typically uses TMA as a source of aluminum (Al), TMA was used as a source of carbon (C) due to the large faction of C in the TMA in this study. H_2 as a reactant gas with a plasma

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power of 300 W and argon as a purge gas and carrier gas for $TiCl_4$ were used in both the Ti and C sub-cycles. In the super-cycle using $TiCl_4$ and TMA as a precursor gas for the TiC film, the $TiCl_4$ exposure time was set to 2 s and three TMA exposure conditions were used: 2 s at 250 °C, 8 s at 400 °C, and 10 s at 500 °C. Various pulse widths of TMA at each deposition temperature were selected to show the linear tendency of the WF versus the deposition temperature. By controlling the number of the iterative super-cycles, the TiC film thickness in each case was set thick enough (approximately 30 nm) to avoid the thickness effects which are observed in thin metal film samples [4]. After the deposition of the TiC films at each temperature, these films were delineated using photo-lithography with a subsequent etching step. The nominal size of the fabricated capacitor was 500 μm × 500 μm to achieve a sufficiently measurable capacitance value. The deposited TiC film thicknesses were confirmed in atomic force microscopy (AFM) and transmission electron microscopy (TEM) images of the patterned TiC films on the SiO_2 layer. The measured thicknesses of the TiC films deposited at each temperature have a sub-10% error range up to 30 nm, i.e., 27.2 nm, 29 nm, and 31.2 nm for TiC samples deposited at 250 °C, 400 °C, and 500 °C, respectively. After 10 min forming gas annealing (FGA) at 400 °C, the WFs of the TiC in a MOS capacitor consisting of a TiC/SiO_2/Si stack were extracted from the measured capacitance–voltage (*C–V*) characteristics.

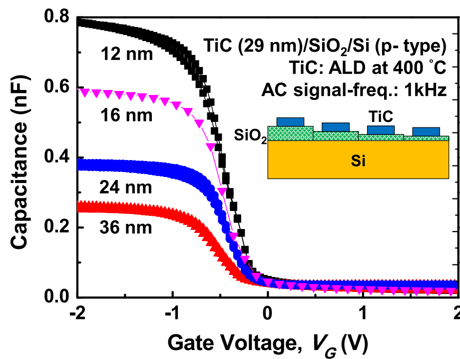

Fig. 1. Typical *C–V* characteristics of devices created at a deposition temperature of 400 °C with various SiO_2 thicknesses ranging from 12 nm to 36 nm.

3. Results and discussion

Fig. 1 shows the typical *C–V* curves of the MOS capacitor for various gate oxide thicknesses ranging from 12 nm to 36 nm when the TiC was deposited at 400 °C. A simplified schematic of the MOS capacitor is illustrated in the inset of Fig. 1. It is important to note that the *C–V* curves in Fig. 1 were randomly overlaid with two data sets deposited and measured at an interval of three months to support WF robustness of TiC films against possible environmental effects and for good long-term durability. The WFs of the TiC films deposited at 250 °C, 400 °C, and 500 °C are 5.24 eV, 4.74 eV, and 4.45 eV, respectively. It should be noted that the tunability of the WF is 0.79 eV. Additionally, the resistivity of TiC film deposited at 500 °C was approximately 450 μΩ cm. Compared to previous reports pertaining to TiN and TiAlN, which are widely used as gate metals, this wide range of WF tunability and the resistivity values of films deposited under different conditions are notably improved. Their enhancement is attributed to the intrinsically outstanding

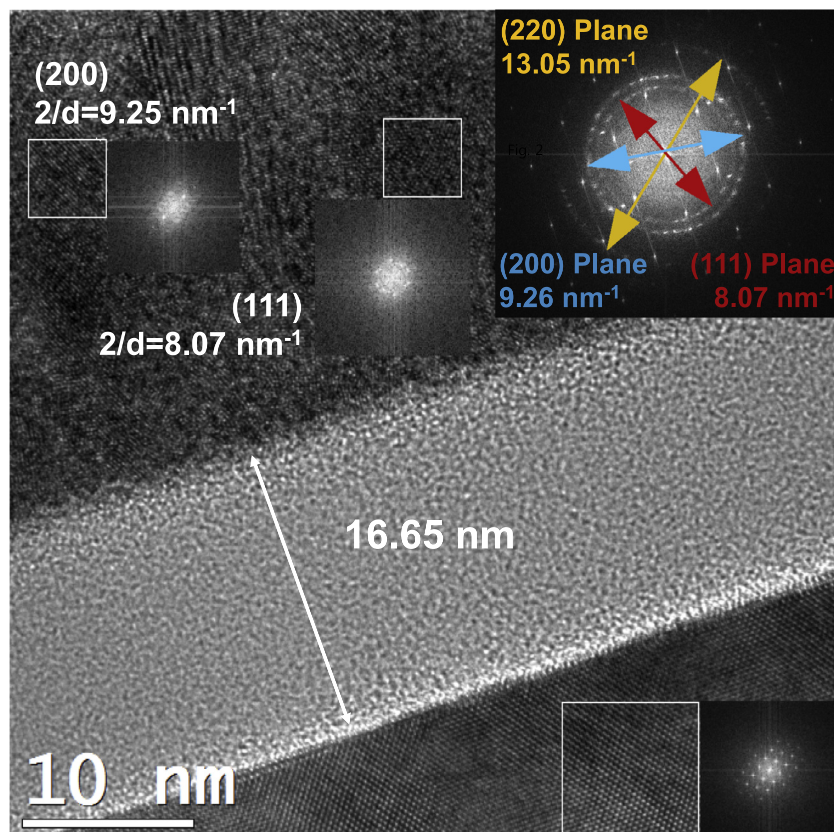

Fig. 2. Cs-TEM image of TiC film deposited on SiO_2/Si at 400 °C by ALD. The fast Fourier transform (FFT) image on the upper-right side of the figure shows the poly-crystalline structure of the TiC film.

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