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Evaluation and optimization of short channel ferroelectric MOSFET for low power circuit application with BSIM4 and Landau theory

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ABSTRACT

Based on BSIM4 parameters of 45 nm metal gate/high-k CMOS process and Landau theory, gate and output characteristics of short channel ferroelectric MOSFET (FeFET) are evaluated to explore its optimal structure for low power circuit application. Unlike previously reported simulation results of long channel FeFET, our work reveals that its current–voltage performance is quite susceptible to the parasitic capacitance between the gate and drain. As a consequence, there is a large threshold voltage increase with drain voltage and output characteristics hardly get saturated, indicating that short channel FeFET is not suitable for analog circuit applications. One effective way to address the issues is to minimize the gate-to-drain parasitic overlap and fringing field capacitances. With the tool Purdue Emerging Technology Evaluator, the inverter performance consisting of modified FeFETs is also simulated. Compared with intrinsic inverter, its energy consumption per cycle is much lower at any supply voltage V_{DD} and the propagation delay is also smaller at very low V_{DD}. Our work shows that the optimized FeFET structure, designed by mitigating gate-to-drain parasitic, is suitable for both analog and digital low power circuit designs.

1. Introduction

As feature size scales down in MOSFET, the rapidly increasing power consumption has become a severe issue that slows down the integration density of transistors on a chip [1]. In order to reduce heat dissipation, abrupt-turn-on devices have been widely investigated to operate at a lower voltage to continue technology evolution according to Moore's law [2,3]. Ferroelectric MOSFET (FeFET) is one of the promising candidates to achieve the abrupt response. It consists of a ferroelectric thin film in the gate stack and an intrinsic MOSFET below. As described by Landau theory, the negative capacitance contribution to the gate stack by addition of ferroelectric can provide internal voltage amplification, resulting in effective sub-60 mV/dec subthreshold swing (SS) [4]. The key to hysteresis-free FeFET design, which is required for analog and digital applications, is capacitance matching: positive capacitance of intrinsic MOSFET below the ferroelectric should stabilize its negative capacitance. To our knowledge, so far the non-hysteretic electrical characteristics can be experimentally observed in ferroelectric-dielectric bilayer [5,6]. Integration of well-known perovskite-type ferroelectrics on intrinsic MOSFET is very challenging due to issues like low-quality interface, mismatch of thermal expansion coefficients between ferroelectric oxide and Si, and incomplete screening, which have not been addressed [7]. Another type of ferroelectric, copolymer P(VDF-TrFE) can be spin-coated on MOSFET [8,9]. However, hysteresis is still inevitable in reported measurements [10–12].

The experiments reported in earlier works [7,10–12] do not give a view of electrical performance in integrated circuits (ICs) using FeFETs. Instead, Landau-based analytical modelling is often used for a reasonable current–voltage prediction [13–15]. However, these simulations are only valid for long channel FeFET, unable to take short channel effects into consideration. Yeung et. al. used Sentaurus TCAD tool to simulate a non-hysteretic short channel FeFET [16]. The key to the ideal structure is to utilize ultrathin Si (0.5–2 nm) as the channel on a thin high-k buried oxide over a degenerately doped Si substrate. However, it is quite difficult to fabricate such thin single crystal Si with high carrier mobility on oxide layer.

In this article, in order to evaluate the integration of ferroelectric on practical short channel bulk CMOS, we simulate its drain current–gate/drain voltage (I_{DS}–V_G/V_D) relationships based on BSIM4 model [17] and Landau theory. Gate and output characteristics are predicted to provide approach and guidelines on structure optimization. In addition, the tool Purdue Emerging

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Technology Evaluator (PETE) [18,19] is used to further discuss inverter performance consisting of FeFETs, including voltage transfer curve, energy consumption per cycle and propagation delay at reduced supply voltage V_{DD}.

2. Device structure

Fig. 1 shows a typical metal-ferroelectric-metal–insulator–semiconductor (MFMIS) structure of FeFET. Its physical model is a capacitive voltage divider. V_{mos} is the internal voltage that appears at the internal gate of intrinsic MOS stack and V_G is the external or applied gate voltage. Gate-to-drain capacitance C_{GD} consists of intrinsic and parasitic ones. The intrinsic capacitance is negligible compared to parasitic capacitance at the saturation region. The parasitic capacitances include contributions from heavily-doped region-gate overlap C_{GDO}, lightly-doped region-gate overlap C_{GDL} and fringing field from gate sidewall C_F. The pair of metals sandwiching ferroelectric layer is quite necessary for perfect screening to suppress depolarization field because it can strongly affect the device stability [20,21] and a multi-domain region would form to minimize total energy and reduce internal voltage amplification [22]. Gate charge density Q_G conservation at the intermediate metal determines potential and field distribution in the ferroelectric layer and MOSFET below it. Landau theory can quantitatively describe the charge–voltage (Q–V) characteristic of ferroelectric [Eq. (1)] and its capacitance [Eq. (2)], where $\alpha(=\alpha_0(T-T_C)\alpha,\ \alpha_0>0$, T_C is Curie temperature) and β are called Landau parameters [3]. For thin film ferroelectric, size effect must be considered, which can be modeled through size dependent values of α and β [23].

$$V_{FE} = V_G - V_{mos} = Et_{FE} = 2\alpha t_{FE} Q_G + 4\beta t_{FE} Q_G^3 \tag{1}$$

$$C_{FE} = \frac{1}{2\alpha t_{FE} + 12\beta t_{FE} Q_G^2} \tag{2}$$

Since short channel FeFET is comprised of intrinsic MOSFET and the stacked ferroelectric in the gate region, its electrical performance can be obtained by separately simulating the two components and linking them together self-consistently through identical charge at the intermediate contact. Q_G–V_{mos}, I_{DS}–V_{mos} and I_{DS}–V_D characteristics of intrinsic MOSFET are simulated in HSPICE with BSIM4 parameters of the given technology node, which includes short channel effects. Then V_G–V_{mos} relationship is derived based on Q_G–V_{mos} characteristic and Eq. (1). Consequently, I_{DS}–V_G and I_{DS}–V_D performances of short channel FeFET are worked out through one-to-one correspondence of I_{DS}, V_{mos} and V_G by finding V_G for every I_{DS}–V_{mos} pair. Such an approach makes calculation of electrical characteristics straightforward although it leads to even scale on I_{DS}–V_{mos} but uneven scale on V_G–V_{mos}.

45 nm metal gate/high-k CMOS process is used in the following simulations [24]. Its key model parameters in BSIM4 are listed in Table 1. Because C_{GDL} is quite small compared with C_{GDO}, only the latter one is included in the overlap capacitance. Fig. 2(a) illustrates gate charge density Q_G–V_{mos} plots under different V_D. Due to C_{GD}, Q_G is also highly dependent on V_D. It will be shortly noted that this effect strongly degrades current–voltage relationship of short channel FeFET. Another important observation from the plot is that Q_G of the two MOSFETs is less than 3 μC/cm^2, which means that ferroelectrics $Pb(Zr_xTi_{1-x})O_3$, $BaTiO_3$ cannot be fully poled as their saturation polarization is much larger. Landau parameters obtained in the major loop of such bulk materials may not be reasonable in this case [25]. Instead, we extract α and β from real measurement. Since P(VDF-TrFE) is the only reported ferroelectric that can exhibit negative capacitance on MOSFET and saturate below 3 μC/cm^2 [10,11], it is used in the following simulation. Red[1] points in Fig. 2(b) are sampled from the experimental result in Fig. 3 of [10]. In order to capture its S-shape P–V or P–E curve, several key points on the experimental curves are selected. Because the negative capacitance value is highly dependent on α at low polarization, the points on the negative-slope curve are selected with a small step (Region A). Points with a positive slope are chosen with a large step to reflect the trend at large polarization, which is determined by β(Region B and B′). For obtaining symmetric P–V relationship, these points have been shifted down by 0.49 μC/cm^2 and right by 0.13 V. By curve fitting, α and β values of P(VDF-TrFE) 70/30 are obtained as -2×10^9 m/F and 7.6×10^{12} m^5/F/C^2, respectively. Fig. 2(b) clearly shows that the black curve plotted using these values of α and β matches well the sampled data, especially around the negative capacitance region of the ascending branch. The slope at each point along the S-shape curve represents ferroelectric capacitance at the corresponding polarization. The negative capacitance regime between the critical polarizations $+P_{cr}$ (0.7 μC/cm^2) and $-P_{cr}$ correspond to identical Q_G range between the dashed lines in Fig. 2(a).

The stability criterion of FeFET is positive total capacitance C_{tot} ($=(C_{FE}^{-1}+C_{mos}^{-1})^{-1}$), which is obtained through minimizing its Gibbs free energy based on Landau theory [26]. However, this method only considers intrinsic capacitances. In short channel FeFET, both intrinsic and parasitic capacitances exist, which means the above criterion could only roughly estimate the upper limit of t_{FE}. The more credible way is to directly simulate I_{DS}–V_G curves of FeFET for different t_{FE}. The result simulated requires that P(VDF-TrFE) layer should be less than 20 nm to avoid hysteresis issue. Such thin film is homogeneous and single domain is highly likely to be formed so that it can be described by Landau theory. The tunneling leakage current through ferroelectric is not considered in our calculation because it can be easily mitigated by appropriately enhancing gate oxide and ferroelectric thicknesses and quality.

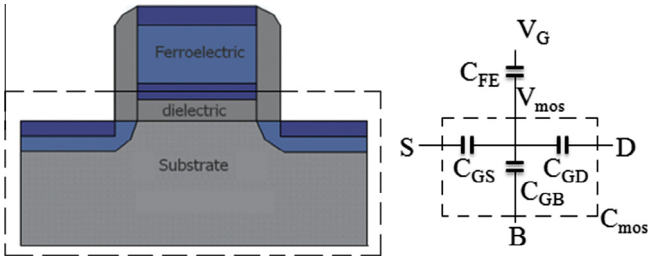

Fig. 1. Metal-ferroelectric-metal–insulator–semiconductor (MFMIS) structure of FeFET and its physical model.

Table 1
Key model parameters of 45 nm n-channel metal gate/high-k bulk CMOS [24].

Technology node	45 nm
Voltage supply V_{DD}	1 V
Threshold voltage V_{th}	0.32 V
Electrical gate equivalent oxide thickness t_{oxe}	0.9 nm
Junction depth X_j	14 nm
Substrate doping N_{sub}	6.5×10^{18} cm^{-3}
Drain junction-to-gate overlap capacitance per channel length C_{GDO}	1×10^{-10} F/m
Fringing field capacitance from gate sidewall C_F	1.1×10^{-10} F/m

3. Electrical characteristics

Fig. 3 shows the electrical characteristics of short channel FeFET (gate length L_G = 50 nm) with 10-nm-thick P(VDF-TrFE) on top. Its

[1] For interpretation of color in Fig. 2, the reader is referred to the web version of this article.