Solid-State Electronics 114 (2015) 115–120

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Bias temperature instability comparison of CMOS LTPS-TFTs with HfO_2 gate dielectric

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ARTICLE INFO

Article history:
Received 21 May 2015
Received in revised form 11 August 2015
Accepted 11 September 2015
Available online 25 September 2015

Keywords:
LTPS-TFTs
HfO_2
PBTI
NBTI
Reliability

ABSTRACT

In this paper, the positive and negative bias temperature instability (P/NBTI) of complementary metal–oxide–semiconductor (CMOS) low-temperature poly-Si thin-film transistors (LTPS-TFTs) with HfO_2 gate dielectric are studied simultaneously. Significant threshold voltage shift ΔV_{TH}, degradation of the sub-threshold swing S.S. and transconductance G_m are observed for both n-type LTPS-TFTs after PBTI stress and p-type LTPS-TFTs after NBTI stress. Moreover, the G_m degradation rate with the stress time of p-type devices during NBTI shows significantly different behavior from the PBTI of n-type devices. The PBTI of n-type device shows a saturation behavior of the G_m degradation with various stress bias and temperature. Conversely, the NBTI of p-type device shows an enhanced G_m degradation rate with the increase of stress time and stress temperature. In addition, the threshold voltage shift $|\Delta V_{TH}|$ of PBTI does not obey the traditional empirical power law model, but the NBTI obeys it with higher time exponent. Consequently, the NBTI of the p-type device shows worse driving current I_{drv} degradation than the PBTI of the n-type device mainly due to the different G_m degradation behavior.

1. Introduction

Low-temperature poly-Si thin-film transistors (LTPS-TFTs) have been widely studied for the application of active matrix liquid crystal display [1], organic light-emitting diode display [2], system-on-panel (SOP) and 3D integrated circuit (3D-IC) [3–5]. The employment of high-κ gate dielectric is a simple way to achieve high electrical performance of LTPS-TFTs without any additional defect passivation process due to its high gate capacitance density [6–8]. Among many high-κ materials, the HfO_2-based materials have been adopted as the gate dielectric of advanced complementary metal–oxide–semiconductor (CMOS) field-effect transistors in very-large-scale integration industry beyond 45-nm node technology [9–11]. However, the reliability of transistors with high-κ gate dielectric is a crucial issue because of the poor high-κ/Si interface and trap states in the high-κ film [12,13]. Therefore, the negative and positive bias temperature instabilities (N/PBTI) are very important for the development of CMOS transistors with high-κ gate dielectric [14]. Nevertheless, the NBTI behavior of p-type LTPS-TFTs and the PBTI behavior of n-type LTPS-TFTs with high-κ gate dielectric have not been simultaneously studied and compared. In this paper, the BTI issues of CMOS LTPS-TFTs with HfO_2 gate dielectric are investigated to observe the degradation behavior and find out the improvement feasibility for the development of SOP and 3D-IC.

2. Experimental procedure

The CMOS LTPS-TFTs were fabricated on Si substrates capped with 500-nm-thick wet oxide. A 50-nm undoped amorphous-Si film was deposited at 550 °C in a low-pressure chemical vapor deposition system, followed by annealing at 600 °C for 24-h to form poly-Si. Then, a 300-nm SiO_2 film was deposited by plasma-enhanced chemical vapor deposition at 300 °C for device isolation. The device active region was created by patterning and etching the isolation oxide. The source and drain (S/D) regions in the active device region were defined by implantation with phosphorus 15 keV, 5×10^{15} cm^{-2} for n-type device and with boron 10 keV, 5×10^{15} cm^{-2} for p-type device. The S/D dopants were activated at 600 °C for 24-h. Then, a 60-nm HfO_2 with effective oxide thickness EOT ~ 12-nm was deposited by a physical vapor deposition (PVD) system at room temperature. After the patterning of S/D contact holes, aluminum was deposited by PVD as the gate and S/D contact electrodes. Finally, the TFT devices were completed by the contact pad definition. The n- and p-type LTPS-TFTs are fabricated on the same wafer. The threshold voltage V_{TH} of n-type and p-type LTPS-TFTs are denoted by V_{THn} and V_{THp}, respectively. They

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http://dx.doi.org/10.1016/j.sse.2015.09.009
0038-1101/

are defined as the gate voltage at which the drain current reaches 10 nA × W/L and $|V_D|$ = 0.1 V. The driving current I_{drv} is defined as the drain current at $V_G - V_{THn} = V_D = 4$ V for n-type device and $V_G - V_{THp} = V_D = -4$ V for p-type device. The electrical measurements are carried out in air by using an Agilent B1500A precision semiconductor parameter analyzer.

3. Results and discussion

The transfer characteristics (I_D–V_G curves) and transconductance G_m behavior of CMOS LTPS-TFTs under NBTI at $V_G - V_{THp}$ = −4 V for p-type device and PBTI at $V_G - V_{THn}$ = 4 V for n-type device with different stress time at T = 75 °C are shown in Figs. 1 and 2, respectively. Significant threshold voltage increase $|\Delta V_{TH}| \sim$ 1.618 V of PBTI and ~1.006 V of NBTI is observed. The threshold voltage shift ΔV_{TH} is defined as the $(V_{THn(after\ stress)} - V_{THn(before\ stress)})$ for n-type device and $(V_{THp(after\ stress)} - V_{THp(before\ stress)})$ for p-type device. In addition, serious subthreshold swing S.S. degradation are also observed that ΔS.S. = 149 mV/decade for n-type device and ΔS.S. = 121 mV/decade for p-type device as shown in Fig. 1. The degradation of subthreshold swing S.S. is attributed to the generation of the interface trap states N_{it} of HfO_2/poly-Si [15–19], which both NBTI and PBTI could degrade the HfO_2/poly-Si interface. In addition, the increase of threshold voltage $|\Delta V_{TH}|$ can be attributed to not only the degradation of subthreshold swing S.S. but also the oxide charge trapping in HfO_2 [19]. The flatband voltage shift $|\Delta V_{FB}|$ of the LTPS-TFTs with undoped poly-Si channel can be used to monitor the threshold voltage shift $|\Delta V_{TH}|$ by the oxide charge trapping, which the flatband voltage V_{FB} is defined as the gate voltage yielding the minimum drain current from the transfer characteristics I_D–V_G curve [16]. As shown in Fig. 1, the flatband voltage shifts $|\Delta V_{FB}|$ of PBTI for n-type device and NBTI for p-type device are around 1.0 V and 0.45 V, respectively. It indicates the electron trapping of PBTI for n-type device is more serious than the hole trapping of NBTI for p-type device, resulting in the main difference of threshold voltage shift $|\Delta V_{TH}|$ between PBTI and NBTI.

In addition to the threshold voltage shift $|\Delta V_{TH}|$ and the subthreshold swing S.S. degradation, the significant difference between NBTI of p-type device and PBTI of n-type device is the transconductance G_m degradation behavior as shown in Fig. 2. The transconductance G_m degradation under NBTI of p-type device is much worse than the PBTI of n-type device, and the G_m degradation of PBTI shows a saturation behavior that NBTI doesn't. In order to confirm this different transconductance G_m degradation behavior of N/PBTI, several stress voltage conditions $V_G - V_{THn}$ = 3 V ~ 5 V and $V_G - V_{THp}$ = −3 V ~ −5 V are executed and the results are shown in Fig. 3(a) and (b). Obviously, higher stress voltage of BTI condition results in more transconductance G_m degradation, but the PBTI of n-type device still shows the saturation behavior of transconductance G_m degradation around 50 s to 100 s of stress time for all stress voltage at T = 75 °C. Conversely, the transconductance G_m degradation of NBTI for p-type device doesn't be saturated with the stress time. Various stress temperatures are also executed and the results are shown in Fig. 4(a) and (b). Higher temperature of PBTI for n-type device shows more transconductance G_m degradation and later saturation time of G_m degradation, and the NBTI of p-type device shows much enhanced degradation rate with the increased temperature. The transconductance G_m of poly-Si TFTs is strongly related to the tail-trap states located near the band edge of poly-Si in the HfO_2/poly-Si interface and the grain boundaries of poly-Si near the surface conduction channel [16–19]. The saturated G_m degradation of PBTI of n-type device indicates the generation of tail-trap states near the conduction band by PBTI is saturated, and the continuous G_m degradation of NBTI for p-type device indicates the generation of tail-trap states near the valence band by NBTI is enhanced. In addition, the subthreshold swing S.S. of poly-Si TFTs is strongly related to the deep-trap states located near the midgap of poly-Si in the HfO_2/poly-Si interface and the grain boundaries of poly-Si near the surface conduction channel [16–19]. Although the transconductance G_m degradation of PBTI for n-type device shows a saturated behavior, the subthreshold swing S.S. degradation of PBTI doesn't, which is shown in Fig. 5. It indicates the generation behavior of tail-trap states and deep-trap states during the stress time of PBTI for n-type device are not equal. The generation of tail-trap states can be saturated and the generation of deep-trap states can't.

The threshold voltage shift $|\Delta V_{TH}|$ of BTI is generally extracted and empirically modeled as following power law equation [20]:

$$|\Delta V_{TH}| \propto t^n \exp(-E_a/kT) \exp(qaE_{ox}/kT) \quad (1)$$

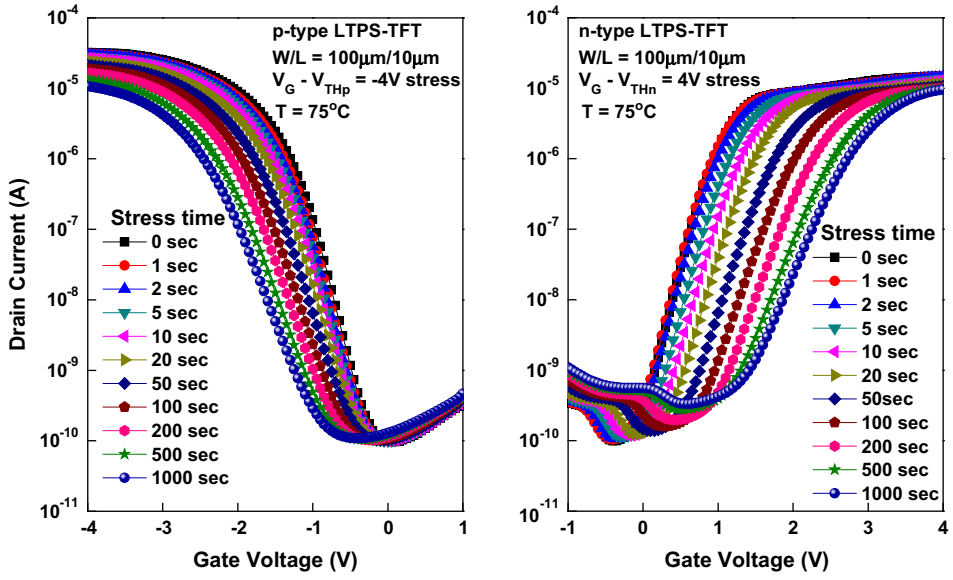

Fig. 1. The transfer characteristics of CMOS LTPS-TFTs under NBTI for p-type devices and PBTI for n-type devices with different stress time.