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Process dependency on threshold voltage of GaN MOSFET on AlGaN/GaN heterostructure

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ABSTRACT

GaN metal–oxide–semiconductor field-effect transistors (MOSFETs) with recessed gate on AlGaN/GaN heterostructure are reported in which the drain and source ohmic contacts were fabricated on the AlGaN/GaN heterostructure and the electron channel was formed on the GaN buffer layer by removing the AlGaN barrier layer. Negative threshold voltages were commonly observed in all devices. To investigate the reasons of the negative threshold voltages, different oxide thickness, etching gas and bias power of inductively-coupled plasma (ICP) system were utilized in the fabrication process of the GaN MOSFETs. It is found that positive charges of around 1×10^{12} q/cm^2 exist near the interface at the just threshold condition in both silane- and tetraethylorthosilicate (TEOS)-based devices. It is also found that the threshold voltages do not obviously change with the different etching gas ($SiCl_4$, BCl_3 and two-step etching of $SiCl_4/Cl_2$) at the same ICP bias power level (20–25 W) and will become deeper when higher bias power is used in the dry recess process which may be related to the much serious ion bombardment damage. Furthermore, X-ray photoelectron spectroscopy (XPS) experiments were done to investigate the surface conditions. It is found that N 1s peaks become lower with higher bias power of the dry etching process. Also, silicon contamination was found and could be removed by HNO_3/HF solution. It indicates that the nitrogen vacancies are mainly responsible for the negative threshold voltages rather than the silicon contamination. It demonstrates that optimization of the ICP recess conditions and improvement of the surface condition are still necessary to realize enhancement-mode GaN MOSFETs on AlGaN/GaN heterostructure.

1. Introduction

Gallium nitride has good characteristics for power devices owing to the high electron saturation velocity and critical electric field [1–3]. In recent years, excellent results have been reported in AlGaN/GaN heterostructure field-effect transistors (HFETs). However, they showed normally-on operation [4,5] which will increase the power consumption of the circuit system. Enhancement-mode (E-mode) operation of FET is required for safe operation and low power consumption [6]. Basically, E-mode operation requires two points: (1) positive threshold voltage and (2) high current conduction at positive gate voltage (high channel mobility).

GaN metal–oxide–semiconductor field-effect transistor (MOSFET) on AlGaN/GaN heterostructure is an interesting candidate for the easy fabrication of source and drain ohmic contacts [7]. In this structure, dry recess process is necessary to remove the AlGaN layer above the channel region. In the latest years, several works have been done to improve the channel mobility of the GaN MOSFETs. Ao et al. reported GaN MOSFETs with silane plasma-enhanced chemical vapor deposition (PECVD) gate oxide and the mobility of 137 cm^2/V s in 2011 [8]. Tsai et al. reported GaN MOSFET with high-k $LaAl_2O_3/SiO_2$ gate dielectric which has high channel mobility of 201 cm^2/V s [9]. Zhang et al. investigated the pyroelectric and polarization effect in GaN MOS diodes and FETs in 2012 [10]. Jiang et al. reported GaN MOSFETs of mobility around 140 cm^2/V s with BCl_3 as the dry etching gas [11]. However, for the recessed GaN MOSFETs or MOS diodes on the semi-insulating GaN

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(SI-GaN), it sometimes shows negative threshold voltages or flat band voltages. Also, the mobility values of them are still too low. They are the problems for E-mode devices [8,10,11], which may relate to the dry process and the charges in the oxide.

In this paper, the performance of GaN MOSFETs with silane- and tetraethylorthosilicate (TEOS)-based gate oxides were evaluated on both channel mobility and interface state density. Then the process dependency, including different oxide thickness and different dry recess process, on the threshold voltage of GaN MOSFET on AlGaN/GaN heterostructure were investigated in detail. The reasons for the negative shift of the threshold voltage were analyzed. Finally, X-ray photoelectron spectroscopy (XPS) experiments were done to confirm the surface damage and contamination on the dry-etched GaN surface.

2. Device structure and fabrication

The structure of the GaN MOSFETs is shown in Fig. 1, which is made on an AlGaN/GaN HFET structure formed on sapphire substrate. To suppress the current collapse effect by the electron injection at the source and drain surface, n-type AlGaN barrier layer and GaN cap layer with doping density of $1 \times 10^{19}\,cm^{-3}$ were used [12]. From top to bottom, the *n*-GaN, *n*-AlGaN and SI-GaN (semi-insulating GaN) layers are with thickness of 10 nm, 20 nm and 2 μm, respectively. The measured sheet resistance of this wafer is about 460 Ω/square which is much lower than that of the wafer without high doping in the cap layers (519 Ω/square) from the same wafer maker.

The fabrication process is based on the standard photolithography and lift-off technologies. After device isolation by inductively coupled plasma (ICP) etching with $SiCl_4$ gas, the 2DEG layer in the channel region was recessed for 40 nm. In this process, different etching gas ($SiCl_4$, BCl_3, and Cl_2) and bias power (20–60 W) were used to investigate the dry recess process dependency on performance of the devices. After that, surface treatment with HNO_3/HF (10 min) was given to remove the possible Si contamination or damage on the etched surface. Then SiO_2 insulator with thickness of 30–100 nm was deposited using plasma-enhance chemical vapor deposition (PECVD) (PD-220LC, SAMCO) with silane and TEOS source, respectively. Then, they were annealed at 1000 °C for 10 min in N_2 ambient which was reported as an optimized annealing condition to minimize the interface state density [3,8,13]. The ohmic contacts were formed using Ti/Al/Ti/Au (50/200/40/40 nm) and annealed at 850 °C for 1 min in N_2 ambient. The evaluation of transmission line model (TLM) showed that the contact resistance was around 0.3 Ω mm. Finally, Ni/Au (70/30 nm) was deposited as the gate metal.

Three types of GaN MOSFETs were designed for device evaluation (Fig. 2), which were long-channel ring-type (W_{eff} = 819 μm, L = 94 μm), long-channel bar-type (W = 200 μm, L = 100 μm), and short-channel bar-type (W = 56 μm, L = 20 μm) MOSFETs.

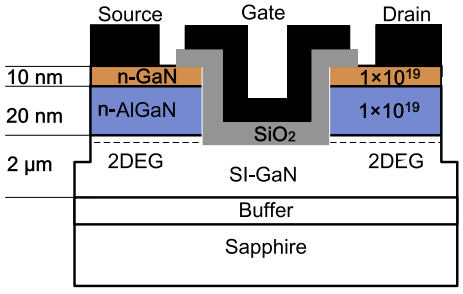

Fig. 1. GaN MOSFET structure on AlGaN/GaN heterostructure.

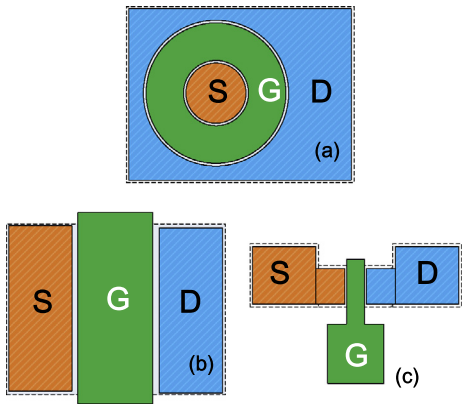

Fig. 2. GaN MOSFET layout. (a) Long-channel ring-type, (b) long-channel bar-type and (c) short-channel bar-type.

3. Device characterization and discussion

3.1. Evaluation of device with silane- and TEOS-based gate oxide

Based on the gradual channel approximation (GCA) model, long channel MOSFETs were utilized for device evaluation in which the effect from the series resistance and the discrepancy of gate dimension between the design and fabrication could be ignored [14]. Instead of the bar-type one, a long-channel ring-type device with inner and outer gate radii of 89 and 183 μm was used to avoid the leakage current from the isolation region.

The current–voltage (*I*–*V*) characteristics of the long-channel ring-type MOSFET with 100 nm silane based oxide is shown in Fig. 3. Device operation up to gate voltage of 10 V was confirmed. Also, hysteresis was not obviously observed. It is possibly due to the use of *n*-GaN/*n*-AlGaN cap layer in the wafer. Fig. 4 shows the transfer characteristics at a drain voltage of 0.1 V. The dry recess conditions of these devices were with ICP/Bias power of 100/20 W, etching gas of $SiCl_4$ and surface treatment of HNO_3/HF (10 min). Threshold voltages of MOSFETs with silane-based oxide of 100, 60, and 30 nm are −3.0, −1.1, and 0.0 V, respectively. For devices with TEOS-based oxide of 30 and 100 nm, the threshold voltages are about −3.0 and 0.0 V, respectively. Fig. 5 is the normalized capacitance–voltage (*C*–*V*) characteristics, showing similar trend of threshold shift with the transfer characteristics in Fig. 4. Fig. 6 shows the typical oxide breakdown properties of both silane- and TEOS-based oxide layers. Since a vertical MOS structure is difficult to realize on the wafer with sapphire substrate, a lateral MOS structure (Fig. 6) was measured in strong accumulation

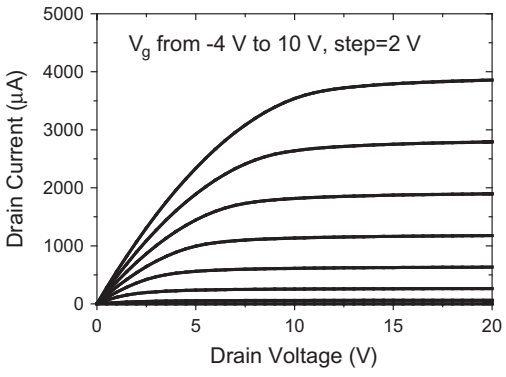

Fig. 3. Current–voltage characteristics of a long-channel ring-type MOSFET with 100 nm silane based oxide.