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Letter

Trans-capacitance modeling in junctionless gate-all-around nanowire FETs

Farzan Jazaeri *, Lucian Barbut, Jean-Michel Sallese

Swiss Federal Institute of Technology in Lausanne (EPFL), 1015 Lausanne, Switzerland

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ABSTRACT

In this brief, we derive an analytical model for trans-capacitances in Junctionless Nanowire Field Effect Transistors (JL NW FET). As for static operation, we show that a complete small signal capacitance network can be built upon an equivalence scheme recently pointed out between JL NW FET and its double gate counterpart for which such a model has been proposed. This approach is validated by 3D Technology Computer Aided Design simulations and bridges the gap between the nanowire junctionless device and its application in circuits.

1. Introduction

Due to relentless downscaling of CMOS technology, more challenges are encountered in order to circumvent fabrication issues of integrated circuits [1]. Junctionless Nanowire Field Effect Transistors (JL NW FETs) such as the Gate-All-Around (GAA) architecture are potential candidates for next-generation high-speed and low-power electron devices owing to their electrostatic integrity and simple fabrication steps, still maintaining acceptable current densities [2–6].

On the other hand, to investigate the performance of integrated circuits built upon JL NW FETs, analytical compact models are needed. In particular, design of analog and digital blocs for low-power and high-performance applications becomes highly dependent on the device small-signal characteristics. This device feature asks for some accurate evaluation of the trans-capacitance matrix. Although there have been many efforts to model DC characteristics of junctionless devices [7–11], a small signal model for JL NW FET is still missing today, mainly because of the quite complex link between charges and potentials for such a cylindrical topology [11].

Conversely, the situation is different for the planar double gate counterpart where a complete trans-capacitance model valid in all the regions of operation, i.e. from deep depletion to accumulation, was recently published [12].

Almost at the same time, a DC model for the JL NW FET which using core relationships of the JL DG FET [7] with equivalent parameters has been evidenced in [13].

Following the same idea, we propose to generalize this correspondence and illustrate how a full trans-capacitance model for the JL NW FET can be mapped upon the AC core developed for the JL DG FET [12] when introducing the equivalent parameters as in [13]. Even though this approach is likely to do the job, it must be proved that it holds for AC analysis, given that dealing with derivatives always generates unexpected mismatch.

Along this brief, we will illustrate how this equivalence is indeed suitable for trans-capacitances when using the compact model in [12]; then, more generally speaking, we will show how this 'mapping' between planar and cylindrical profiles is featured by TCAD simulations only, i.e. how this 'correspondence' is 'intrinsic' and not related to any compact models.

2. Modeling capacitances in JL nanowire with equivalent JL DG FET parameters

2.1. Equivalent parameters definition

The 3D schematic of the JL NW FET is shown in Fig. 1a. Here, L_G and $t_{ox} = R_2 - R_1$ represent the gate length and gate oxide thickness;

* Corresponding author. Tel.: +41 216934603.
E-mail address: Farzan.jazaeri@epfl.ch (F. Jazaeri).

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R_1 and N_D are the semiconductor radius and the dopant density in the channel. As proposed in [13], the strong similarities which exist between double gate and JL NW FETs inspire to use the same set of charge–voltage relationships for both architectures to establish a compact model for the trans-capacitances in JL NW FETs. Following the charge-based approach proposed in [7,13], new equivalent model parameters for the DG counterpart as given in Table 1 have to be used, together with the equivalent oxide thickness for the DG which is given by [13]:

$$t_{OX}^{Eq\_DG} = \frac{T_{SC}}{2}\ln(1 + 2t_{OX}/T_{SC}), \quad (1)$$

where T_{sc} is given by $2 \times R_1$ and ε_{ox} is the oxide permittivity. Therefore, considering the JL NW FET structure as a JL DG FET as sketched on Fig. 1 and using the so-called equivalent parameters (see Table 1), a complete description of charges inthe JL NW FET can be obtained from the charge-based model in [7]. Note that since the silicon thickness is greater than 10 nm, quantum mechanical effects have not been included in the model [14–17]. A correction has been proposed recently for inversion mode DG FETs by [17] which could apply to JL DG FET as well.

As stated in [13], the main relationships derived for the JL DG FET case can be used to obtain the mobile charge density at source and drain ($Q_{m,s}$ and $Q_{m,d}$) and also at specific internal points along the channel (see (8), (9), (12), and (13) in [12]), which is required to calculate the partitioning for the mobile charge density [18]. Following this approach, the trans-capacitance matrix for the JL NW FET can then be calculated in the general case, with matrix elements defined as $C_{ij} = \partial Q_{m,i}/\partial V_j$. Here, $Q_{m,i}$ is global source and drain charge densities, as defined in [12,18], and V_i is the gate or drain-to-source potential. Given that the source node is used as the reference for the potentials, only six trans-capacitances exist, namely C_{GG}, C_{GD}, C_{DG}, C_{SG}, C_{SD}, C_{DD}.

2.2. Simulations and discussion

Considering an n-type JL NW FETs with $N_D = 2 \times 10^{19}$ cm^{-3}, $R_1 = 5$ nm, $L_G = 100$ nm, and $t_{ox} = 1.5$ nm, the six trans-capacitances (abs. val.) versus the gate voltage dependence obtained from TCAD simulations are plotted on Fig. 2 (red dots), both for $V_{DS} = 0$ V and $V_{DS} = 1$ V (respectively in Fig. 2a and b).

Similarly, trans-capacitances obtained from the analytical model developed in [12] including the equivalent double gate parameters are shown in full line.

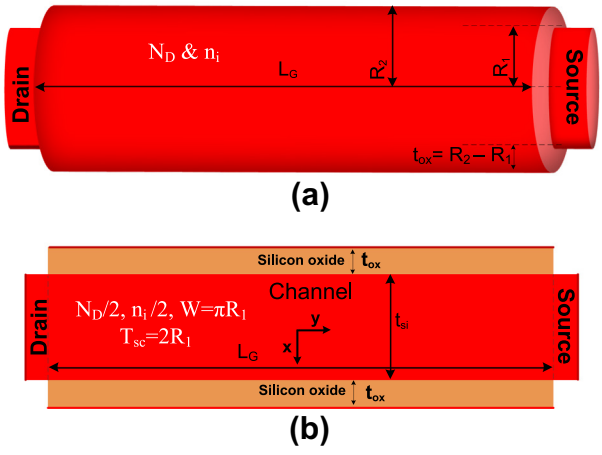

Fig. 1. Schematic view of then-type JL NWFET (a) and its equivalent JL DG FET structure (b).

Table 1
Correspondence between nanowire physical parameters and equivalent DG FET model parameters [13].

Physical parameters	Nanowire	Equivalent DG FET
Radius and thickness	R (radius)	$T_{sc} = 2 \times R$
Oxide thickness	t_{ox}	$T_{sc}/2 \times \ln(1 + 2t_{ox}/T_{sc})$
Width	– –	$W = \pi \times R$
Doping concentration	N_D	$N_D/2$
Intrinsic carrier concentration	n_i	$n_i/2$

The agreement between the numerical calculations and the equivalent JL DG FET compact model are quite good, this is particularly true when considering linear operation. Considering higher drain voltage, the matching happens to be slightly degraded, but the model is still able to give a good estimation of the different capacitive components. Given that we are dealing with derivatives which magnify any mismatch, these results underline the soundness of the DG versus NW correspondence as far as capacitances are concerned.

Trans-capacitances in a wider NW having $R_1 = 10$ nm, $N_D = 1 \times 10^{19}$ cm^{-3}, $L_G = 100$ nm, and $t_{ox} = 1.5$ nm are also shown in Fig. 3a and b, still for $V_{DS} = 0$ V and $V_{DS} = 1$ V. Similarly, we obtain a good prediction of the matrix capacitance for the JL NW adopting the JL DG FET model [12].

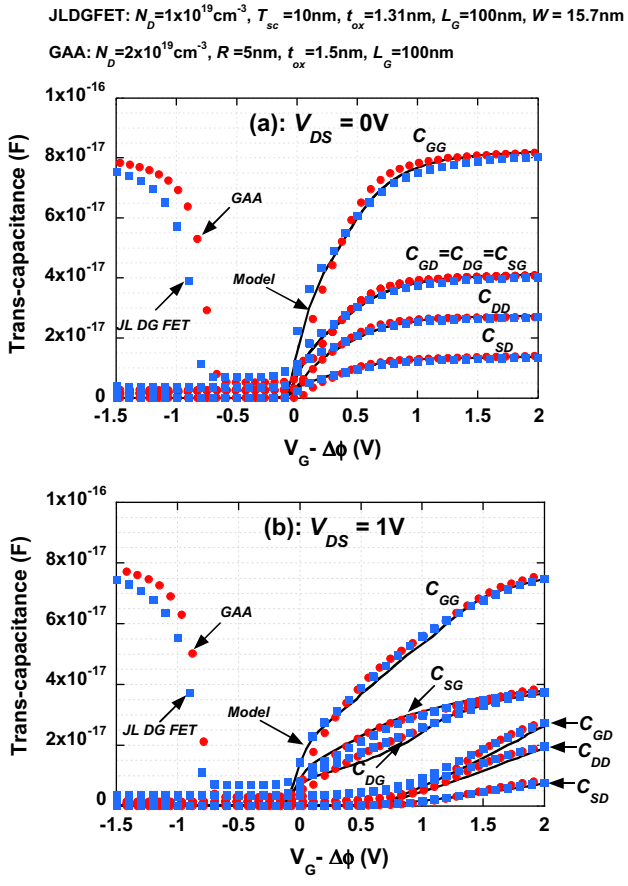

Fig. 2. Dependence of the trans-capacitance versus the gate voltage ($V_G - \Delta\varphi$) for $V_{DS} = 0$ and 1 V shown in (a) and (b) respectively. Lines and symbols are for the analytical model and TCAD simulations respectively. Red dots and blue squares are respectively for TCAD simulations of GAA JL NW FET ($N_D = 2 \times 10^{19}$ cm^{-3}, $R_1 = 5$ nm, $L_G = 100$ nm, and $t_{ox} = 1.5$ nm) and the equivalent JL DG FET device ($N_D = 1 \times 10^{19}$ cm^{-3}, $T_{sc} = 10$ nm, $L_G = 100$ nm, and $t_{ox} = 1.31$ nm). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)