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Effect of In addition and annealing temperature on the device performance of solution-processed In–Zn–Sn–O thin film transistors

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ABSTRACT

We fabricated solution-processed thin film transistors (TFTs) with an In–Zn–Sn–O (IZTO) channel layer and investigated the effect of In addition on the device performance of IZTO TFTs. Also, in order to examine the dependence of electrical characteristics on microstructural evolution of a channel layer, annealing temperatures were varied from 400 to 600 °C. With an increase of In content in IZTO films, the off-current was increased and threshold voltage was shifted to the negative direction. This was due to the increase of carrier concentration caused by In addition. For the samples annealed below 500 °C, amorphous phases were obtained. In contrast, for the sample annealed at 600 °C, nanocrystalline films were obtained. With increasing annealing temperature, on/off current ratio and saturation mobility were increased because the quality of IZTO films was improved by phase transformation from amorphous to nanocrystalline phase.

1. Introduction

Transparent oxide-based thin film transistors (TFTs) have attracted significant attention because of their potential applications for many electronic devices such as active matrix liquid crystal displays (AMLCDs), organic light emitting diodes (OLEDs), and see-through displays [1,2]. Oxide semiconductors have an advantage of high mobility and transparency when compared to an amorphous Si (a-Si) used as a TFT channel layer. There are many oxide semiconductors including ZnO [3], InZnO (IZO) [4], ZnSnO (ZTO) [5], and InGaZnO (IGZO) [6,7]. Among them, IGZO is presently the most preferred material due to its high mobility (>10 $cm^2/V\,s$) and outstanding electrical stability. However, In and Ga are rare and expensive elements. So, it is required to study a channel layer based on oxide semiconductors without In and Ga or with fewer elements. For this reason, several studies on ZTO channel layers have recently been reported [5,8–10].

In order to improve the device performance of ZTO TFTs, some studies of adding a suitable metal component have been carried out. Especially, it is well known that if metal elements such as Ga [11], Hf [12], Zr [13], Ti [14], and Mg [15] were added in ZTO, off-current was decreased and stability under bias stress and light illumination was improved because the metallic atoms added were strongly bonded to oxygen atoms, leading to the reduction of oxygen vacancy, which acts as a carrier source in a channel layer. Recently, an effort to improve the carrier mobility in a channel layer is emerging as a major issue. It was reported that when In was added in ZTO, the mobility of the channel layer are increased and the threshold voltage was shifted in the negative direction [16,17]. However, nanocrystalline quaternary InZnSnO (IZTO) system has rarely been studied.

Oxide semiconductors can be fabricated using a solution process, which can replace a vacuum deposition method due to its simple and low-cost processing. Additionally, it can be applied for printed electronics such as an inkjet printing [18]. It is presently reported that the high performance TFTs having oxide semiconductor channels such as ZnO [19], IZO [20], IGZO [21], and ZTO [22] were fabricated using solution process. However, the solution-processed TFTs exhibited the instability under positive bias stress (PBS) and light illumination [23]. This limits the practical application due to the absence of reproducibility and reliability. The suitable metallic components such as Ga [24] and Mg [15] have been added to the ZnO-based TFTs in order to improve the bias stress instability.

In this paper, we fabricated the TFTs with sol–gel processed IZTO channel layers and investigated the microstructure of the channel layers and the electrical characteristics of TFTs with varying the In content. The device performance of IZTO TFTs with increasing annealing temperature was also examined. The

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comparison between the device performances of TFTs with nanocrystalline or amorphous channel layer was performed.

2. Experimental details

In order to fabricate the IZTO films, the metal precursor solution was prepared with indium acetate [$In(C_2H_3O_2)_3$], 0.1 M zinc acetate [$Zn(C_2H_3O_2)_2$], and 0.2 M tin chloride dihydrate [$SnCl_2{\cdot}2H_2O$]. 2-methoxyethanol [$C_3H_8O_2$] was used as a solvent and ethanolamine [C_2H_7NO] of 1/20 solvent volume was used as a stabilizer to maintain the solution homogeneous. The concentration of Zn and Sn cations was fixed at 0.3 M. The In contents added were 0.01, 0.03 and 0.05 M. The solution prepared was stirred with 300 rpm for 1 h on a hot plate.

The insulating SiO_2 with a thickness of 100 nm was thermally grown on heavily doped p^+-Si as a gate dielectric. The metal precursor solution was filtered through a 0.22 μm syringe filter and deposited on the substrate by the spin-coating method at 4000 rpm for 30 s in N_2 ambient. After the deposition of IZTO films, the drying process was performed at 150 °C for 1 h in air ambient to remove the solvent. Then, the heat treatment was conducted to get rid of organic compound in films and to make a dense film through calcination and sintering effect. The heat treatment was performed from 400 to 600 °C at increments of 100 °C with a tube furnace in air ambient. After the annealing of IZTO films, the 150 nm-thick Al film was deposited as a source and drain electrode by using a dc sputter with a shadow mask. The channel width and length were 500 and 100 μm, respectively.

X-ray diffraction (XRD; D/Max-2500, Rigaku Japan) and transmission electron microscopy (TEM; Tecnai G2 F20 S-TWIN, FEI, USA) measurements were performed so as to investigate the crystal structure and microstructural properties. The electrical characteristics of IZTO TFTs were characterized with a semiconductor parameter analyzer (Agilent 4156C).

3. Results and discussion

Fig. 1 shows the XRD patterns of ZTO and IZTO films annealed at 500 °C as a function of In content. The thickness of the films was approximately 35 nm, which was confirmed by TEM results. There are no remarkable peaks for the ZTO sample without In content. On the other hand, with increasing the In content added, several weak halo peaks were observed. This means that the IZTO films were amorphous or nanocrystalline phases when they were annealed under air atmosphere at 500 °C.

Fig. 2 is the output curves of ZTO and IZTO TFTs annealed at 500 °C as a function of In content, where the gate voltage was varied from 0 to 40 V. When the In content was increased to 0.03 M, the output curves showed the distinct linear and saturation region. When the drain voltage (V_D) increased, the drain current (I_D) began to linearly increase and then saturate to a certain value. This pinch-off phenomenon confirms that the TFTs with IZTO channel layers were normally operated. When the In content was 0.05 M, the good device performance was not obtained (not shown here).

Fig. 3 shows the transfer curves of ZTO and IZTO TFTs annealed at 500 °C as a function of In content at a drain voltage of 30 V. With increasing the In content, both on- and off-current increased due to the increase of the carrier concentration caused by the In addition, which acts as a carrier source. The saturation mobility (μ_{sat}) was obtained from the slope of the square root of I_D versus V_G and the threshold voltage (V_T) of the devices was calculated by extrapolating the linear region of the curve to $I_D = 0$ using the following equation [14].

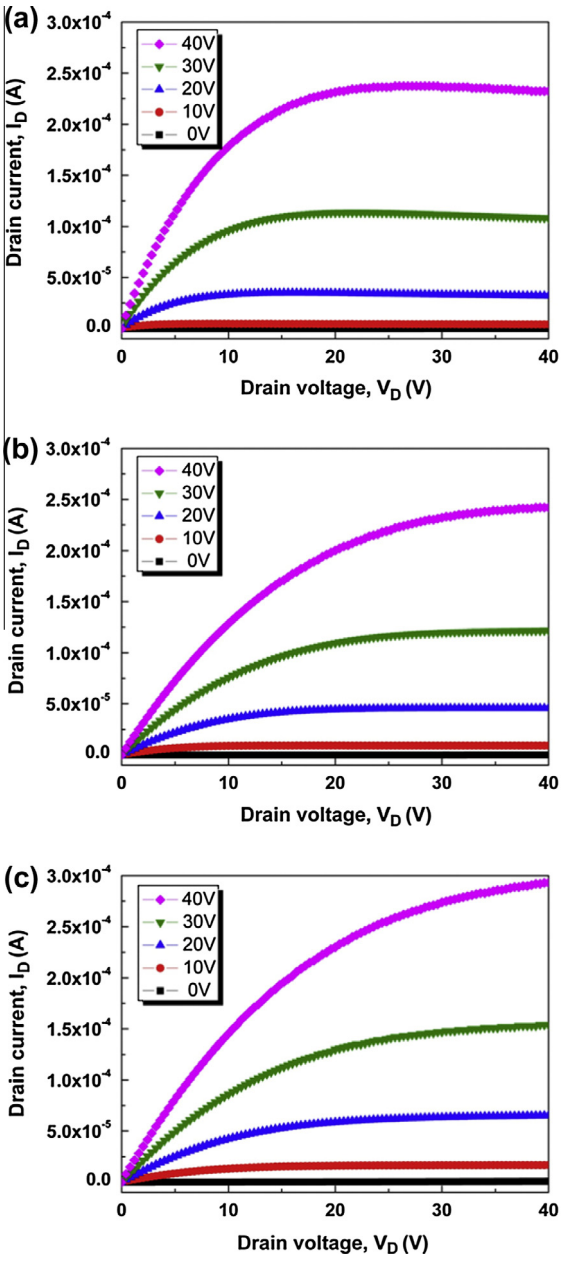

Fig. 2. Output curves of IZTO TFTs with different In contents: (a) 0, (b) 0.01, and (c) 0.03 M.

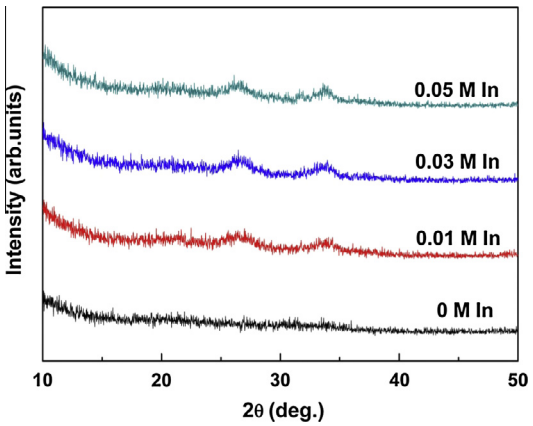

Fig. 1. XRD patterns of IZTO thin films as a function of In content.