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Low-frequency noise and effective trap density of short channel p- and n-types junctionless nanowire transistors

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ABSTRACT

This work presents an evaluation of the Low-Frequency Noise (LFN) exhibited by short-channel Junctionless Nanowire Transistors (JNTs). Unlike in previous works in which only the noise of n-type transistors was evaluated, this paper exhibits an analysis of both the LFN and the effective trap density of n- and p-type JNTs. The low-frequency noise is analyzed in terms of the channel length as well as doping concentration and has shown to be nearly independent on the former parameter when the device is biased above threshold and to decrease with the raise of the latter. Also, carrier number fluctuations dominate the LFN in nMOS JNTs whereas an important mobility fluctuation component is present in the pMOS ones. The effective trap density of JNTs has shown to be in the order of 10^{19} cm^{-3} eV^{-1}, presenting its maximum around 1.4 nm away from the silicon/gate dielectric interface independently on the device type or doping concentration.

1. Introduction

Multi-gate architectures are one of the most attractive to the fabrication of transistors in ultimate technological nodes (22 nm and below) [1]. The presence of a gate that covers more than one side of the channel region improves the electrostatic coupling between gate and channel, making multi-gate devices less susceptible to the occurrence of short-channel effects (SCEs). The formation of p–n ultra-sharp junctions between source/drain and channel, however, consists in an important issue for the fabrication process of inversion mode (IM) multi-gate transistors, such as tri-gates, of extremely reduced dimensions, since the thermal and doping conditions must be precisely controlled to avoid the source/drain dopants diffusion into the channel region.

A novel device so-called Junctionless Nanowire Transistor (JNT) presents a constant and heavy doping concentration ($\sim 10^{19}$ cm^{-3}) from source to drain, intrinsically eliminating diffusion-related problems [2–4]. The longitudinal sections of both a triple gate inversion mode transistor and a triple gate JNT are shown in Fig. 1. Contrarily to FinFETs and other IM transistors, JNTs are accumulation mode devices, in which the off-state is reached through the full depletion of the silicon at low gate biases (V_{GS}) guaranteed by the different workfunctions between gate material and silicon. Above threshold, the depth of the depletion region induced by the gate is reduced and a neutral path is formed deep in the silicon giving rise to a bulk current [5]. Several advantages in favor of JNTs have been recently reported in terms of Drain Induced Barrier Lowering (DIBL), subthreshold slope and analog properties [6,7].

The Low-Frequency Noise (LFN) is an important parameter which not only can limit the output signal of an analog system, but also allows for the investigation of gate dielectric integrity. The LFN of JNTs has been addressed in different papers [8–13] in the last years. Refs. [8–11] only evaluate the LFN of n-type devices, whereas Ref. [12] addresses the noise of both p- and n-type JNTs without evaluating the dielectric integrity. In [13], the effective trap density presented by JNTs has only been evaluated for n-type devices with different gate stacks.

According to [10,11], the LFN exhibited by n-type JNTs can be up to five orders of magnitude lower than IM transistors of similar dimensions and can be partially explained by the smaller current presented by such devices with respect to inversion mode ones. However, the noise studies performed in [8–12] present some discrepancies on LFN origin and its dependence on the frequency (f). Refs. [8,9,12] show that the noise of n-type JNTs can exhibit either $1/f$ or $1/f^2$ behavior depending on the samples and on the gate and drain biases whereas in [10] only a surprisingly weak $1/f$ is observed independently on biases and samples.

This paper presents, for the first time, an in-depth evaluation of the LFN resultant from both n- and p-types short channel junctionless nanowire transistors. The analysis is carried out in terms of doping concentration (N_A in pMOS and N_D in nMOS, respectively),

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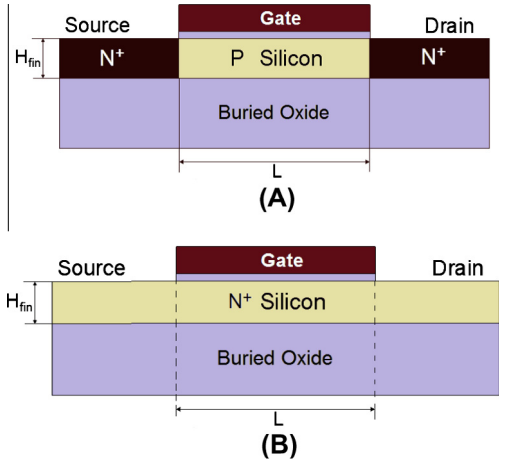

Fig. 1. Longitudinal section of (A) an inversion mode transistor and (B) a junctionless nanowire.

channel length (L) and voltage bias aiming at pointing out the noise origins.

2. Devices characteristics

JNTs studied along the work were fabricated on standard SOI substrates and present 50 parallel fins with effective width (W_{fin}) of 20 nm each and silicon layer thickness of 10 nm, as described in [14]. Devices with different channel lengths (50 and 100 nm) and doping concentrations (0.5 and 1×10^{19} cm^{-3}) were evaluated. The gate stack is composed by SiO_2/HfSiON followed by TiN and polysilicon, which results in an effective oxide thickness of 1.5 nm. The application of a midgap material with workfunction around 4.7 eV in the gate allowed for the adjustment of the threshold voltage (V_{TH}) to suitable values. The longer devices with doping concentration of 5×10^{18} cm^{-3} have presented $|V_{TH}|$ around 0.45 V whereas the short channel ones present $|V_{TH}| \approx 0.35$ V. By increasing the doping concentration to 1×10^{19} cm^{-3}, a reduction of about 250 mV was obtained in $|V_{TH}|$ for all the devices. Also, the subthreshold slope was extracted for all devices and showed values around 65 mV/decade, ensuring the silicon is fully depleted in subthreshold region.

3. Low-frequency noise analysis

The LFN presented by most MOS transistors is commonly attributed to the trapping and release of carriers near the interface between silicon and gate dielectric. However, in partially depleted SOI devices, part of the excess noise is correlated to defects in the silicon layer as stated in [15]. According to [9], the overall LFN of JNTs is determined by a mutual contribution between both mechanisms due to JNTs peculiar conduction mode, in which bulk current is dominant at low V_{GS} and accumulation current prevails above flatband [5]. Also, the high ion implantation dose required to attain the desired doping concentration in the channel of JNTs can increase the defects in the silicon layer degrading the LFN [9].

The curves of the current noise spectral density (S_{Id}) as a function of the frequency of both n- and p-type junctionless nanowires have been extracted and are presented in Fig. 2 for transistors with $L = 100$ nm and doping concentration of 5×10^{18} cm^{-3} biased at drain voltage (V_{DS}) of 0.1 V for gate biases from below threshold up to gate voltage overdrives ($|V_{GT}| = |V_{GS} - V_{TH}|$) of 0.6 V, with steps of 100 mV. It can be seen that, mainly at higher V_{GT}, p-type devices present lower LNF than n-type ones, which is related to

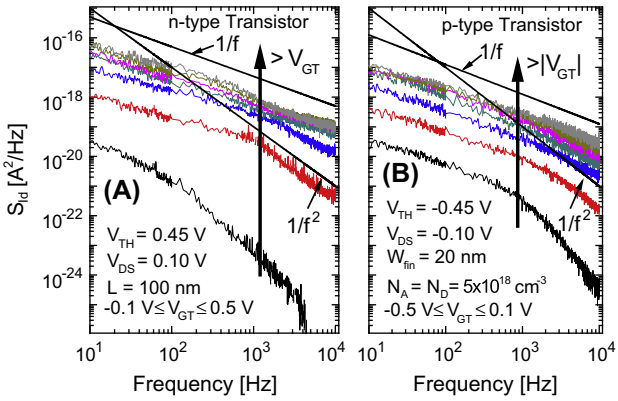

Fig. 2. Current noise spectral density (S_{Id}) as a function of the frequency for (A) n-type and (B) p-type junctionless nanowire transistors with $L = 100$ nm, $W_{fin} = 20$ nm and $N_A = N_D = 5 \times 10^{18}$ cm^{-3} biased at $|V_{DS}| = 0.1$ V.

their reduced drain current (I_{DS}) at a similar $|V_{GT}|$, resultant from the lower mobility presented by holes.

Junctionless nanowires can exhibit either $1/f$ or $1/f^2$ behavior, depending on the gate bias and frequency. Independently on the device type, the LNF presented by JNTs biased above V_{TH} exhibits $1/f$ behavior at lower frequencies and $1/f^2$ at higher ones. The latter is treated as Lorentzians [16] and is frequently associated to generation–recombination (g–r) centers. The dependence of the Lorentzian corner frequency on V_{GT} (Fig. 2) indicates that the g–r centers are placed within the gate dielectric [17]. The $1/f^2$ noise presented in the evaluated devices is lower than the one shown in [9], which addresses the LFN of JNTs fabricated in a different gate stack technology (10 nm-thick SiO_2 layer). As stated in [13], devices fabricated with SiO_2 gate dielectric present lower overall noise being more susceptible to Lorentzians. The shape of the current noise spectral density is not significantly impacted when varying L or $N_{A,D}$.

When evaluating the overall noise as a function of $|V_{GT}|$, it can be noted that any increase in $|V_{GT}|$ seems to raise S_{Id} up to $|V_{GT}| = 0.2$ V. For higher gate overdrive voltages, saturation on the overall noise is observed for both devices and is related to the formation of a superficial accumulation layer when the transistors reach the flatband limiting the trapping/release of carriers. The flatband voltage of the n-type devices takes place around $V_{GS} = 0.65$ V (V_{GT} around 0.30 V) [18].

As p- and n-type devices present different I_{DS} at a similar V_{GT} due to the dissimilar mobility of electrons and holes, the intrinsic LFN of a transistor (independently on the current level) can only

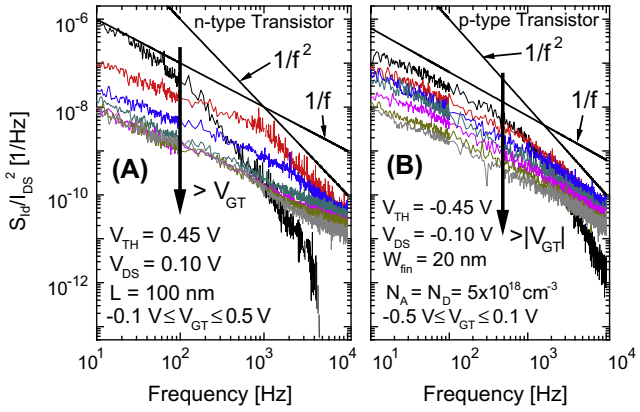

Fig. 3. Current noise spectral density normalized by the square of the drain current (S_{Id}/I_{DS}^2) as a function of the frequency for (A) n-type and (B) p-type junctionless nanowire transistors with $L = 100$ nm, $W_{fin} = 20$ nm and $N_A = N_D = 5 \times 10^{18}$ cm^{-3}.