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Trigger voltage walk-out phenomenon in SOI lateral insulated gate bipolar transistor under repetitive electrostatic discharge stresses

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ABSTRACT

Trigger voltage walk-out phenomenon is found in SOI LIGBT's under repetitive ESD stresses. Such a characteristic would cause an IC to be susceptible to the risk of exceeding the ESD design window and thus resulting in core circuit damages when the LIGBT is served as an ESD protection device in the SOI process. This trigger-voltage walk-out phenomenon is investigated in this paper, and both the experimental evidences and device simulation results are presented to offer the insight of the underlying physical mechanism.

1. Introduction

Silicon-on-insulator (SOI) lateral insulated gate bipolar transistors (LIGBT's) have been frequently used in high-voltage (HV) power IC's because of its complete dielectric isolation, low on-state resistance, high operational voltage, and compact size. In the HV IC's, the electrostatic discharge (ESD) protection is always an important and challenging issue [1–3]. Lately, there have been some interests in the SOI LIGBT for high-voltage ESD applications, due to its intrinsic PNPN SCR-like structure and robust current handling ability [4–7]. However, as will be shown later, such a device is prone to trigger-voltage increase after repetitive ESD stresses, a phenomenon called "the trigger-voltage walk-out" that can give rise to the internal circuit failure under ESD stresses.

Several investigations have been reported that the trapping of hot electrons at the Si/SiO_2 interface is responsible for the trigger-voltage walk-out phenomenon in drain extended MOS and SCR devices [8,9]. This paper offers the underlying insight into the physical mechanism of the trigger-voltage walk-out observed in the SOI LIGBT device by means of measurements and TCAD simulations.

2. Experimental results and analysis

2.1. Structure and operation principle

The LIGBT under study is fabricated in a 0.5 μm, 5 V/160 V SOI process, and is used as output stage in a plasma display panel (PDP) scan driver IC. Its cross-section view is shown in Fig. 1. The poly gate length is 8 μm and the effective channel length (Lch) is 1 μm. The drift region of N-Epi can be divided into two parts: the accumulation region with a length Lacc = 2.5 μm and the field oxide region with a length Lfox = 16.5 μm. The buried oxide (BOX) thickness is 1 μm, and the silicon film thickness is 9 μm. The Si/SiO_2 and Si/BOX interfaces are marked in the figure. Due to the large areas in the power IC, the LIGBT acts as ESD device for self-protection, as shown in Fig. 2. Under ESD stress condition, the high electric field in the LIGBT would cause junction breakdown and trigger the parasitic SCR (P+_N-Epi_P-Body_N+) structure. Thanks to the high current handling capability and snapback characteristic associated with the SCR, the ESD current could be discharged via the LIGBT with a low clamping voltage and high robustness.

2.2. Trigger voltage walk-out phenomenon

The transmission line pulsing (TLP) tester which can generate pulses with a pulse width of 100 ns and a rise time of 10 ns is

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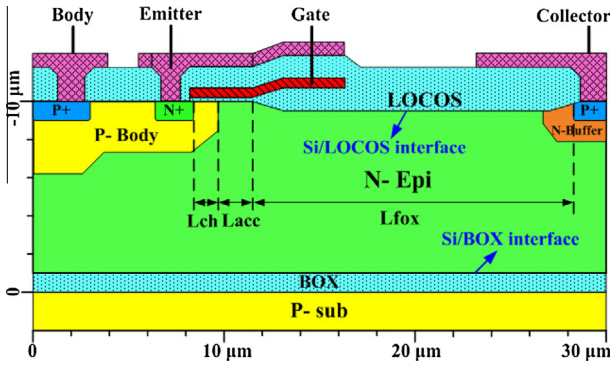

Fig. 1. Cross-section of the investigated LIGBT structure.

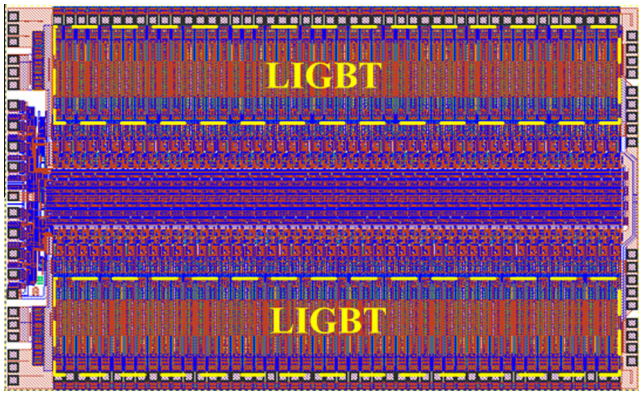

Fig. 2. The layout of plasma display panel (PDP) scan driver IC.

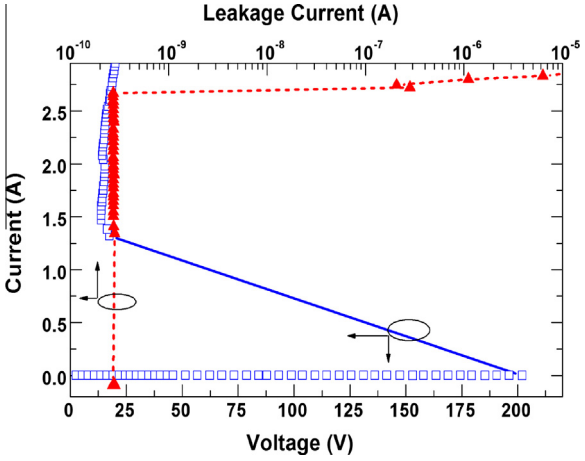

Fig. 3. Measured TLP *I–V* characteristic of SOI LIGBT.

utilized to characterize the LIGBT under the ESD stress. Fig. 3 shows the TLP *I–V* curve of the gate-grounded LIGBT. Breakdown occurs when the voltage is increased up to 200 V, followed up by a snapback. With device width of 60 μm, the failure current (It2) can be as high as 2.7 A, this correlates to a high human body model (HBM) passing voltage of 4 kV.

For many high-voltage ESD devices, their ESD performance often is degraded when subjecting to repetitive stresses [10]. The SOI LIGBT is zapped by repetitive TLP stresses with the current level below It2 so that the device is not damaged during the TLP testing. Fig. 4 shows the TLP *I–V* curves as a function of the zapping times. The time interval between the successive zaps is 3 s. Clearly,

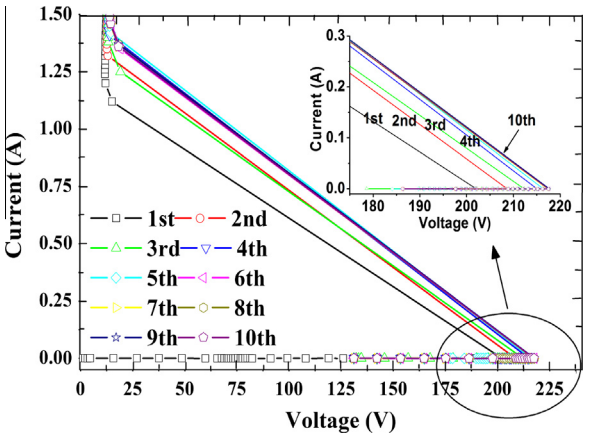

Fig. 4. Measured *I–V* curves of SOI LIGBT subject to repetitive TLP stresses.

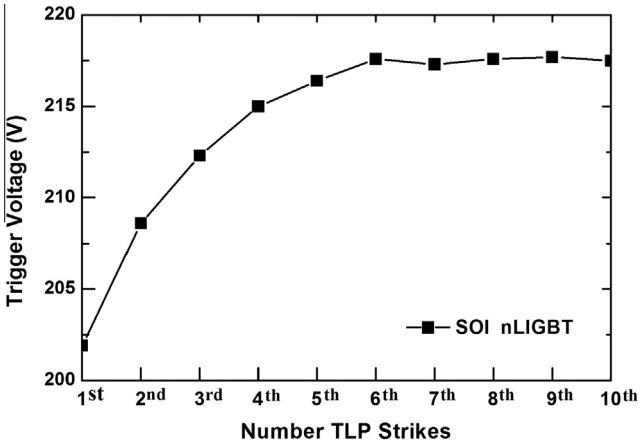

Fig. 5. Trigger voltage evolution as a function of the TLP zapping time.

the trigger voltage walk-out is prominent in the SOI LIGBT, and the trigger voltage increases from 201.9 V to 217.6 V after six repetitive stresses. Beyond this point, the trigger voltage becomes saturated vs. the zapping time, as illustrated in Fig. 5. The leakage current varies only slightly with the number of zapping.

2.3. Simulations and analysis

Two-dimensional TCAD electro-thermal simulations are carried out to provide insights into the trigger voltage walk-out behavior of the LIGBT under the ESD stress.

High electric fields take place at the Si/LOCOS and Si/BOX interfaces, and simulated electric field distributions along these interfaces under the breakdown condition are shown in Fig. 6. At the Si/LOCOS interface, three electric field peaks are observed at the bird's beak regions near the emitter, right edge of the polysilicon, and the left edge of the metal collector. At the Si/BOX interface, the electric field peak exists in the region underneath the collector, and this is the maximum electric field in the whole device. As such, the breakdown point is located at the Si/BOX interface underneath the collector.

Fig. 7 shows the hole current contours and electric field vectors during the breakdown condition. In consistent with the electric field vectors, the hole current first flows vertically through the N-Epi/BOX/P-Sub junction, and then the current flows horizontally along the Si/BOX interface.

High impact ionization rate is always associated with the high electric field, as evidenced by the results in Fig. 8. It is clear that