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Effects of shallow trench isolation on low frequency noise characteristics of source-follower transistors in CMOS image sensors

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ABSTRACT

The effects of the shallow trench isolation (STI) edge on low frequency noise characteristics of source-follower (SF) transistors in CMOS image sensors (CIS) were investigated. Random telegraph signal (RTS) noise and 1/f noise were measured in a CIS operating voltage region for a realistic assessment. SF transistor with STI edge in contact with channel shows a lower probability of generating RTS noise but greater RTS amplitude due to the enhanced trap density induced by STI-induced damage. SF MOSFETs without STI exhibit a much lower 1/f noise power spectral density in spite of the greater RTS generation probability, which is due to the decreased trap density. Therefore, SF transistors without STI edge in contact with channel are promising candidates for low noise CIS applications.

1. Introduction

Due to the recent advances in CMOS technology along with the shrinking of pixel size in MOSFETs, CMOS image sensors (CIS) are being widely used in various image sensor applications. However, the continuous scaling down of CMOS image sensors has incurred undesirable characteristics, particularly random telegraph signal (RTS) noise, which has become one of the major issues in CIS. It is well known that RTS noise is related to a single trap in the Si–SiO_2 interface or SiO_2 bulk [1,2]. 1/f noise is also an important factor in CMOS image sensors. As a result, noise characteristics have become one of the critical factors for high performance CIS. For a conventional 4T CMOS image sensor, system noise is influenced by the noise characteristics of the transistor, especially by the SF transistors, meaning noise can be improved by reducing noise in the SF transistor [3–5]. Therefore, many noise reduction techniques have recently been investigated and applied [4–11]. However, some techniques were the circuit level approach [7,9,10] and there were no mention of the noise characteristics on the device itself. The effect of LOCOS on RTS noise is also proposed [8]. The technique to avoid the channel of the MOS transistor to be in contact with the isolation is similar but the stress between STI and LOCOS process is quite different, which can show different behavior of RTS noise and 1/f noise as will be shown later. Although the STI effect on LFN performance of MOSFETs has been reported [11,12], few publications addressed the STI effect on LFN in CIS and RTS data such as RTS noise event probability and amplitudes have not been addressed.

In this paper, the low frequency noise (LFN) characteristics of source-follower (SF) transistors with and without STI edge in contact with channel are analyzed in depth. To analyze the STI effects on LFN, two kinds of source-follower structures with and without STI were designed and compared.

2. Device structure and experiments

Fig. 1(a) shows the schematic diagram of a SF transistor designed without (WO) STI under the gate. Active region is defined larger than the source/drain region (white area in Fig. 1(a)). Then the source/drain area is formed by the n^+ doped region marked as green region, then the STI edge does not touch the gate oxide edge and source/drain area. A conventional SF transistor with (W) STI was also prepared as a reference as shown in Fig. 1(b). The source/drain region of conventional SF transistor is formed by STI isolation. Thus the gate oxide edge is affected by the STI process. Although the proposed SF transistor WO STI seems larger than a conventional transistor, the pixel size is designed to be

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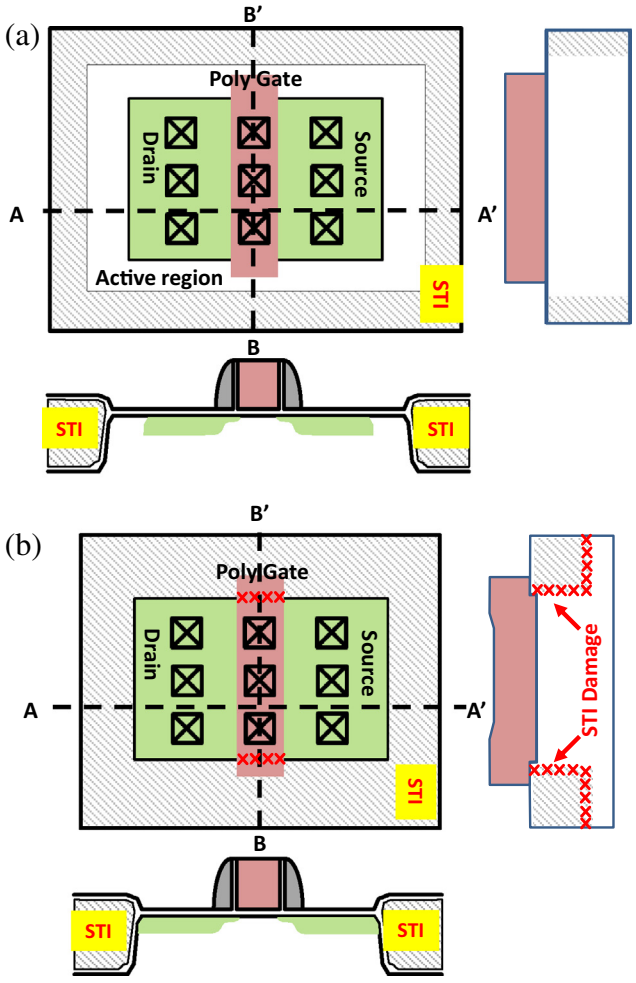

Fig. 1. Schematic diagrams of SF transistors. (a) Proposed structure without STI (WO STI) edge and (b) conventional (W STI) transistor. The STI edge is located far from the source/drain and gate for the proposed structure.

the same. Proposed SF transistors WO STI under the gate were fabricated using a 0.11 μm CMOS image sensor technology. SF transistors 0.3 μm wide and 0.4 μm long were used for the experiment.

A parameter analyzer (Agilent 4156C) was used as the DC source and a low noise current preamplifier (SR 570) was used to amplify the drain noise current [14]. The drain current RTS noise and flicker noise were monitored by a dynamic signal analyzer (HP35670A). A low pass filter (AdMOS 1 Hz filter) was used to minimize external noise components [14]. RTS noise and flicker noise in the SF transistors were measured under their actual read-out operation condition (V_G@I_D = 1 μA) in a CIS. We measured 30 samples for the statistical analysis (Full map). Then among the samples which show the RTS noise characteristics are used for the analysis. The wafer we used for this experiment has about 35 dies and on the view of in-wafer variation, 30 samples are enough for having statistical meaning. A cumulative probability curve and a box chart were used for statistical analysis of the drain current RTS noise and flicker noise.

3. Results and discussion

Fig. 2(a) and (b) display the drain current versus gate voltage characteristics. MOSFETs without STI show lower threshold voltage and also have interestingly lower saturation current. Fig. 2(b) shows the drain current versus gate voltage characteristics under

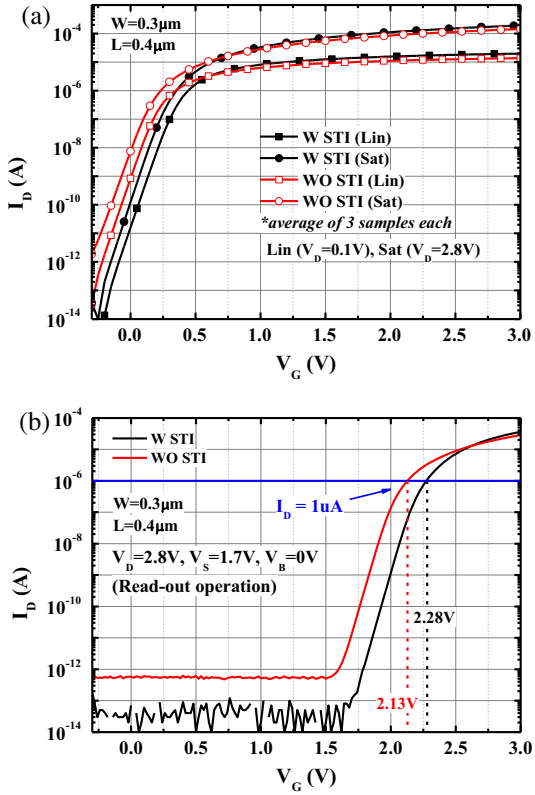

Fig. 2. DC characteristics of MOSFETs with and without STI. (a) drain current versus gate voltage (I_D–V_G) characteristics of linear and saturation and (b) drain current versus gate voltage characteristics under read-out operation condition (V_D = 2.8 V, V_S = 1.7 V and V_B = 0 V).

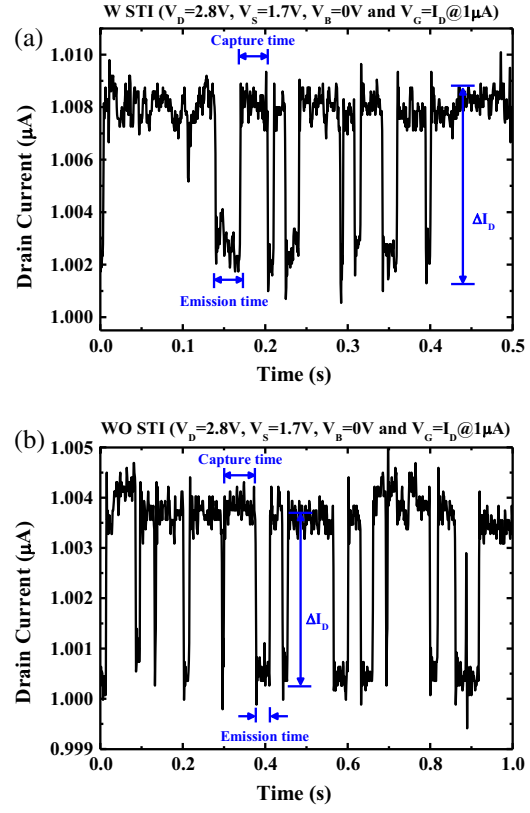

Fig. 3. Measured time domain data of random telegraph signal noise under read-out operation condition. (a) MOSFET with STI and (b) MOSFET without STI.