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A circuit model for defective bilayer graphene transistors

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ABSTRACT

This paper investigates the behaviour of a defective single-gate bilayer graphene transistor. Point defects were introduced into pristine graphene crystal structure using a tightly focused helium ion beam. The transfer characteristics of the exposed transistors were measured ex-situ for different defect concentrations. The channel peak resistance increased with increasing defect concentration whilst the on–off ratio showed a decreasing trend for both electrons and holes. To understand the electrical behaviour of the transistors, a circuit model for bilayer graphene is developed which shows a very good agreement when validated against experimental data. The model allowed parameter extraction of bilayer transistor and can be implemented in circuit level simulators.

1. Introduction

The high electron mobility and saturation velocity in graphene makes it suitable for analogue electronics applications despite the lack of an energy band gap [1].

However, despite the absence of a bandgap in large scale graphene, the long mean free path of electrons and the high carrier mobility allows circuits to operate at high frequencies. Following the achievement of impressive GHz cut-off frequency for graphene transistors [2–4], a number of applications in RF electronics have been reported which include frequency mixers and multipliers [5–7] and oscillators [8]. Equally, a graphene based integrated circuit consisting of active and passive components in the signal amplification, filtering and downconversion mixing units has been demonstrated [9].

The mean free path is limited by the presence of charged impurities (such as trapped charges in the underlying substrate), structural defects, corrugation, etc., which cause scattering of charge carriers. Experimental evidence shows that pristine suspended graphene has an exceptionally high carrier mobility as the substrate effects are eliminated [10,11]. Although carrier transport properties in graphene are well understood, practical models which are useful for circuit level simulation are still lacking. In this work, we systematically investigate the transport characteristics of a pristine bilayer graphene transistor subjected to a deliberate introduction of point defects with precise defect concentration. We subsequently derive a circuit model for the defective graphene transistor which can be embedded in commercial circuit simulators such as Pspice.

2. Graphene device fabrication

Our bilayer graphene exfoliated from graphite (NGS Naturgraphit, GmbH) on a 300 nm-thick silicon oxide, which sits on a highly doped silicon substrate. The bilayer nature of our graphene flakes was determined using Raman spectroscopy and by measuring the intensity of the green component (which allows the best contrast relative to the SiO_2 layer) in RGB images taken by an optical microscope [12]. The graphene channels were fabricated using electron beam lithography and oxygen plasma etching. To contact the BGFET channels, we used Au and Ti (95 nm/5 nm) to define electrodes which were fabricated using electron beam lithography and a liftoff process. The device principal is sketched in Fig. 1. Prior to any electrical measurements using an Agilent B1500A Semiconductor Device Analyser, the BGFETs were annealed at 350 °C for several hours to eliminate atmospheric contamination.

The irradiation with helium ions He^+ was performed in high vacuum inside a helium ion microscope (Zeiss Orion) [13–16]. The acceleration voltage used was 30 kV whilst the current was kept at 1 pA. To avoid variations of contact resistance, contacts were not exposed to the He^+ beam and only graphene channels were irradiated. This was possible by the high precision patterning

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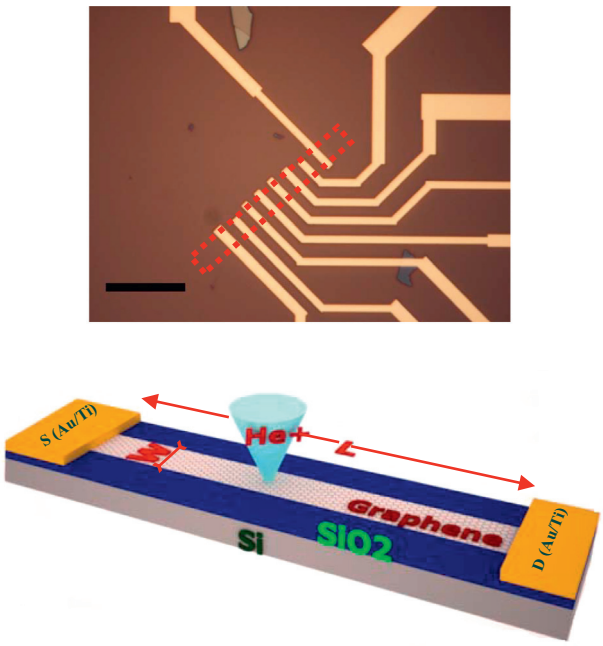

Fig. 1. The sketch of the device showing the BGFET channel, the radiating focused helium ion beam, the source, the drain and the dimensions of the channel. The highly doped silicon substrate is used as a control gate. The inset shows various transistors with different widths situated within the dashed area, and source and drain contacts. The scale bar is 15 μm.

offered by the helium ion microscope, with a He^+ beam spot size of 0.7 nm. The channels were perfectly mapped using an embedded pattern generator. The measurement were performed immediately after each irradiation run. The channels were exposed to doses of 1.5×10^{13} ion/cm^2, 2.35×10^{13} ion/cm^2 and 4.15×10^{13} ion/cm^2. The estimated defect concentration corresponding to these doses are $n_d = 6 \times 10^{10}$ defect/cm^2, 9.4×10^{10} defect/cm^2 and 1.66×10^{11} defect/cm^2 respectively [17,15].

3. Capacitance model

By taking into consideration the geometric structure of the BGFET, a circuit-level schematic is shown in Fig. 2. Here, C_e is the gate dielectric capacitance, C_o is the interlayer capacitance, C_q is the quantum capacitance, R_s is the contact resistance and R_q is the off-current resistance. Although both contacts are expected to have different resistances during conduction, for simplicity, an equal resistance is used.

In this work, the graphene layers are identified based on their proximity to the gate terminal. The layers are numbered in ascending order starting with the layer closest to the gate. On each layer a quantum capacitance, C_q, is present, this is a measure of the energy required to pump carriers into the channel [18]. Hence, it is a derivative of the net charge in the channel to the potential of the channel.

The varying quantum capacitance with surface potential is [19]

$$C_{qvar} = q^2 \frac{2}{\pi} \frac{q|\varphi_s|}{(\hbar v_f)^2} \tag{1}$$

where φ_s is the potential difference between the channel and the source terminal, V_s, v_f is the Fermi velocity [20], electronic charge q and the reduced Plank's constant $\hbar$. The bilayer transistor is modelled as two single layers coupled together by capacitance C_o. As such Eq. (1) is applied to both layers of the transistor. At charge neutrality when the density of states vanishes, a minimum carrier density, n_0, results in a capacitance

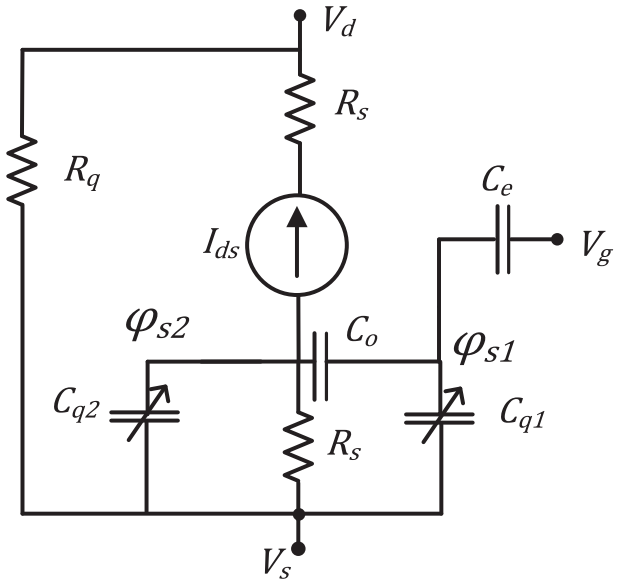

Fig. 2. Equivalent circuit-level diagram for a single gate graphene field effect transistor. Where R_q is the off-current resistance, R_s is the contact resistance, C_q, C_o and C_e are the quantum capacitance, the interlayer capacitance and the gate capacitance respectively, φ_s is the surface potential and V_s, V_g and V_d are the source, gate and drain voltages respectively.

$$C_{qmin} = \frac{q^2\sqrt{n_0}}{\sqrt{\pi}\hbar v_f} \tag{2}$$

Published works report a minimum carrier sheet density in the vicinity of 0.5×10^{12} cm^{-2} at the Dirac point [21,2]. Hence, by applying the Drude model, the quantum capacitance, C_q, takes into consideration the capacitance due to both the minimum charge and the induced charge into the channel [22,23]. Thus, Eqs. (1) and (2) can be algebraically added to give

$$C_q(\varphi_s) = \frac{C_{qmin}^2 + C_{qvar}(\varphi_s)^2}{\sqrt{C_{qvar}(\varphi_s)^2 + C_{qmin}^2}} \tag{3}$$

Since graphene transport is governed by charged impurities, the Drude-Boltzmann model presents a good understanding of the channel conductivity at high charge densities [24,25]. The Drude model is used to evaluate the charge density in the channel using the relation $n = \sqrt{n_0^2 + n[V_g]^2}$, where $n[V_g]$ is the charge density due to the action of the gate potential and n_0 takes into consideration the residual charge in the channel at the Dirac point.

Since the transistor layout has only one gate, it will have only one threshold voltage, V_o. From Eq. (4), this threshold voltage is the gate potential at which the surface potential, φ_{s1} is zero.

$$V_{gs} - V_o = \varphi_{s1}\frac{C_o + C_e + C_{q1}}{C_e} - \varphi_{s2}\frac{C_o}{C_e} \tag{4}$$

The surface potentials of all layers are zero at the charge neutrality point, CNP. This implies that the threshold voltage cannot be optimised [23,12]. Graphene FET threshold voltage is still widely researched [26], whereby it has been reported that chemical doping of the graphene channel can result in a shift of the threshold voltage [26].

As the action of the gate both electrostatically dopes the channel and modulates the doping intensity, both the surface potential