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Flexible thin-film transistors on planarized parylene substrate with recessed individual backgates

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A B S T R A C T

With novel design and fabrication techniques, InGaZnO-based thin-film transistors with individual recessed back-gates were fabricated on flexible and transparent polymer substrates. The key components for the fabrication include using a machine park optimized for Si process technology, low-adhesion, room temperature parylene coating, AlOx–ZnOx(Al)-based inorganic lift-off process, and a recessed individual gate concept. Transistors were built to validate the viability of the design as well as aforementioned techniques. The demonstrated approach could open up new design possibilities for cheap, flexible devices, while the recessed-gate concept shows promise towards the use of more brittle layers in our flexible thin-film electronic devices.

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1. Introduction

Current generation flexible electronics are highly motivated by disposable, low cost, low power purposes in order to achieve a cheap and environmentally friendly array of thin-film devices [1–3] for robotics [4], antenna [5] and display technology [6] or sensory applications.

To achieve such good performance with said devices, it is essential to have good film flexibility while keeping layer homogeneity as ideal as possible. Specifically, it is important to minimize gate leakage [7] and avoid stack cracking under mechanical load [8–10], where both are highly affected by surface particle concentration and the lacking planarization of the substrate surface [11–13].

For sensory applications in particular, a back-gate device configuration is of high relevance in order to expose the sensitive channel region of a thin-film transistor (TFT) to the environment to monitor [14–17]. Furthermore, individual back-gates are necessary for TFT arrays in order to realize desired functionalities such as parallel sensing and addressing.

Unfortunately, when individual back-gates are used, increased surface roughness gets introduced by the gate material stacks, especially if the stacks have certain limitations regarding their thickness. This problem can be the most pressing when brittle layers like graphene [18,19] are considered in a transistor design [20]. Surface roughness can also affect the uniformity of spin-coated materials [21].

To address such issues arising mainly from the aforementioned problem, an individual recessed-gate concept is conceived, following a similar process reported previously [22]. This concept is represented by a device structure where a gate-stack of tens of nm-s is encased into an underlying substrate so as to assure a planarized surface upon completion of the stack formation. Since mounting such advanced design on flexible substrates is also desirable, the substrate/casing material also needs to be flexible, chemically inert and, if possible, transparent. Above all, both the substrate, as well as the design, have to be compatible with a machine park optimized for laboratory scale Si processes.

These challenges have motivated the current work with a demonstration of recessed individual back-gate TFT-s fabricated on flexible and transparent substrates utilizing thin film processes developed for Si technology.

2. Materials and methods

2.1. The recessed-gate concept

The concept's main purpose is to define a masking structure on the substrate, then use the same masking for the plasma etching as

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well as the lift-off process. Following the sketch on the flowchart of Fig. 1, it starts with the deposition of the mask, consisting of two layers (step **A**). This is followed by standard photolithography and subsequent photoresist (PR) removal to define the desired mask arrays with wet etch. The difference in etch rate is used to achieve a proper undercut (step **B**). Casing definition is then accomplished by means of plasma-assisted directional etching (step **C**). A metal is now deposited by electron beam evaporation to fill up the casing (step **D**). Lifting off the lower of the two masking layers closes the whole process, leaving behind a planarized substrate with individual gate metal stripes recessed into the substrate (step **E**).

To implement the flow in Fig. 1, after various tests, a novel aluminum oxide (AlOx) in combination with aluminum-doped zinc-oxide (ZnOx(Al)) masking was developed. While oxygen plasma is generally used to remove polymers, it has little impact on such oxides. Further, the ZnOx(Al) layer can be easily etched in 4% HCl bath, making it ideal for lift-off purposes. The patterning of the mask stack could be done using a 1:80 H_2O:BHF (buffered hydrofluoric acid) wet etch, keeping all tested polymers intact.

As the flexible substrate for the casing, parylene is chosen, since it is chemically inert, transparent and compatible with ultrahigh vacuum processes. In addition, in can withstand 150 °C without any permanent structural damage, yielding a large process window for the device fabrication. It can be etched with low power oxygen plasma, further decreasing the chances for mask degradation. Parylene is also available as a low adhesion glass coating, hence a properly sized substrate carrier could also avoid most of the general flexible substrate handling issues, such as sample bending, heat extension. It also prevents any mechanical incompatibility with the machine park. Finally, parylene itself is cheap to produce.

2.2. Transistor design

The transistor design is sketched up on the flowchart in Fig. 2. The process starts with the coating of a 7 μm thick Galaxyl C (purchased from Galentis Srl.) parylene layer (step **I**) at room temperature on a glass carrier sheet in a Paratech Lab Top 3000 coater. Then (in step **II** as well as later on in steps **VII** and **X**), a 50 W Ar–O_2 plasma of the composition of 6:14 sccm is applied for 1 min in a Plasma Ecth PE-100. For inorganic masking (step **III**), 200 nm thick ZnOx(Al) is sputtered on the samples with a Von Ardenne CS600 sputter, then another 200 nm AlOx layer e-beam evaporated by a Kurt J. Lesker Company PVD75 evaporator. Following is the photolithography (step **IV**), where, immediately after the hexamethyldisilazane (HMDS) priming was applied on the samples to improve photoresist patterning during the pattern definition, S1813 (from Shipley) photoresist is spin coated on the substrate (5000 rpm, 1 μm thickness), then soft baked on 100 °C for 30 min. Patterning is done in a Karl Süss MA6 mask aligner. Next is a 1:80 H_2O:BHF etching (for 4–5 min) to define the undercut for the lift-off (step **V**) using the PR of the previous step as the masking. Stripping of the S1813 is done in ultrasonic acetone bath

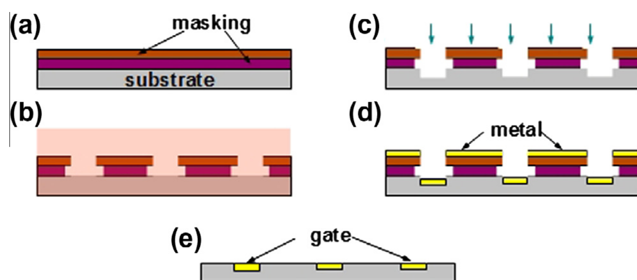

Fig. 1. The recessed-gate concept.

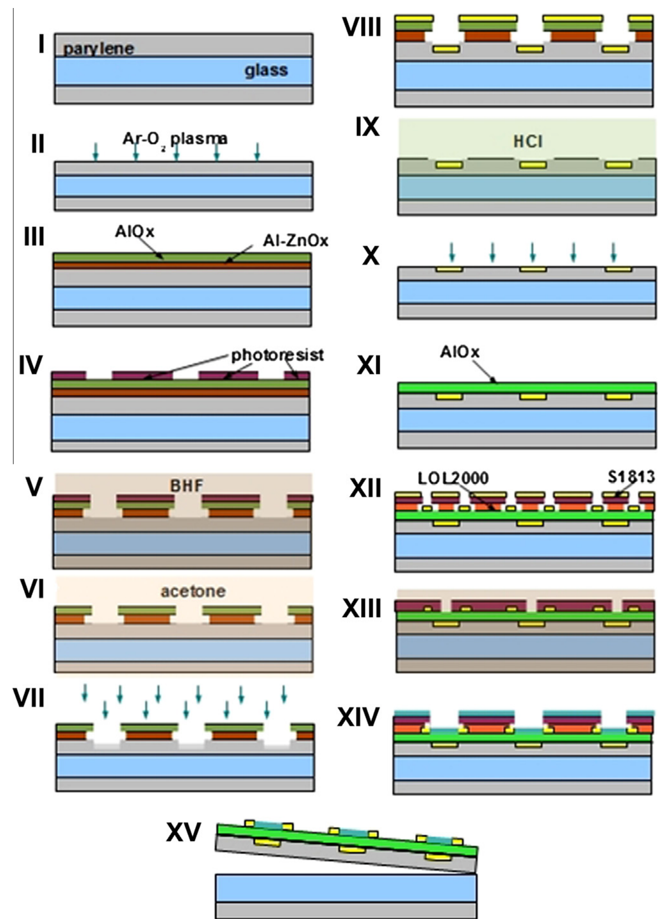

Fig. 2. The recessed-gate process.

(step **VI**). An iso-propanol bath is applied after to clean the surface. As gate, a layer of 10 nm of titanium is e-beam evaporated to prevent gate peel-off, followed by 60 nm resistively evaporated Au from 99% Au pellets in the Lesker PVD75 (step **VIII**). Lift-off (step **IX**) is achieved by a 1 min ultrasonic bath in 4% HCl. After a 1 nm of Al deposition (in PVD75) to improve the nucleation of AlOx, 90 nm thick AlOx is deposited as gate dielectric on the samples with atomic layer deposition (step **XI**).

All remaining steps utilize thin film processes based on Si technology (Ti/Au evaporation in PVD75, S1813-LOL2000 lift-off, BHF wet etching) to fabricate/define the source-drain, the gate contact window and the channel in steps **XII**, **XIII** and **XIV** respectively. In steps **XII** and **XIV**, the LOL2000 photoresist is spin coated with 5000 rpm to get a thickness of 100 nm, then baked under 150 °C for 30 min. The semiconducting InGaZnO (IGZO) is RF-sputtered from an IGZO target on the surface (step **XIV**) with 0.1 sccm O_2, 35 sccm Ar plasma on 10 mTorr pressure and 70 W power for 40 min, resulting in a film thickness of around 40 nm. Film uniformity is achieved by a rotating substrate holder. To conclude the process, the polymer substrate is removed from the glass (step **XV**).

Except for the parylene coating, all fabrication steps are done in clean room environment.

3. Results and discussion

3.1. Discussion of the transistor design

The low power plasma etch of steps **II**, **VII** and **X** was mainly chosen to improve stack adhesion to the parylene as well as to

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