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# Compact core model for Symmetric Double-Gate Junctionless Transistors

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ABSTRACT

A new charge-based compact analytical model for Symmetric Double-Gate Junctionless Transistors is presented. The model is physically-based and considers both the depletion and accumulation operating conditions including the series resistance effects. Most model parameters are related to physical magnitudes and the extraction procedure for each of them is well established. The model provides an accurate continuous description of the transistor behavior in all operating conditions. Among important advantages with respect to previous models are the inclusion of the effect of the series resistance and the fulfilment of being symmetrical with respect to drain voltage equal to zero. It is validated with simulations for doping concentrations of $5 \times 10^{18}$ and $1 \times 10^{19}$ cm$^{-3}$, as well as for layer thickness of 10 and 15 nm, allowing normally-off operation.



## 1. Introduction

Nanowires operating as MOS transistors, where the source and drain regions have the same doping type and concentration of the channel region are known as junctionless transistors (JLT). This type of transistors, proposed in 2009 [1], can be fabricated in a similar way as FinFET transistors without the ion implantation in source/drain and using heavily doped channel layer to improve the device conductance. A detailed theoretical description of this device can be obtained in [2], a study of the effect of channel width on JLT characteristics is described in [3] and the variation of performance with scaling in [4].

Different models for JLT parameters and regions have been presented, for example, in [5] for the threshold voltage model and a model for subthreshold region [6].

A good model for current–voltage characteristics is always required for the application of these devices, reason why different papers have presented approximate numerical–analytical and analytical models [7–12]. In all these papers different approximations are considered for mobile charges in the depletion and accumulation regions, obtaining approximate *I–V* characteristics. The main problem for JLT modeling is the transition from the depletion mode of operation to the accumulation mode, because the physical behavior in both regions is different. In JLTs the conductions at the center of the silicon layer in depletion is larger than at the surface interface, (dielectric-semiconductor) when the device is in subthreshold or in the vicinity of the threshold voltage. For larger gate voltages the accumulation at the interfaces takes place and the conduction occurs not only through the silicon volume but also in the interfaces. A first approach for modeling Symmetric Double-Gate Junctionless Transistors uses only one approximate expression to calculate the expression for the surface-center difference of potential, which was obtained and validated in [13] for different concentrations and silicon layer thicknesses.

In this work an analytical model without any other additional approximation is presented for long channel devices and constant mobility that also considers the series resistance. This model can be considered a core model, where the reduction of fin height, short-channel effects and other effects will be included using the standard procedure of complementing the current–voltage expressions.

In order to validate the new model 2D ATLAS [14] simulations were done for a channel length of 1 μm and three different transistor structures, having positive threshold voltage. The transistors had: channel doping concentration, $N_D$, of $5 \times 10^{18}$ cm$^{-3}$ and silicon layer thickness, $t_S$, with 10 and 15 nm, and $N_D = 1 \times 10^{19}$ cm$^{-3}$ with $t_S = 10$ nm.

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## 2. Model description

### 2.1. Potentials

The analyzed JLT long channel double gate structure is shown in Fig. 1, in which the majority carriers are present in the whole silicon layer, considered the transistor channel. The general expression to calculate the charge density in *N*-type silicon layer with doping concentration $N_D$, including the electron mobile charge, is:

$$\rho = qN_D\left(1 - e^{\frac{\varphi - V}{\varphi_t}}\right), \tag{1}$$

where $\varphi_t = kT/q$ is the thermal potential at temperature $T$; $\varphi_S$ is the surface potential and $V$ is the potential drop across the silicon layer, from source $V_S = 0$ V to drain $V_D$. The reference voltage is considered at the middle of the bad gap.

At the same time in the silicon layer of thickness $t_S$, the surface electric field is calculated solving Poisson equation, under the condition of zero electric field at the center of the silicon layer:

$$E_S = \varphi_t \frac{C_{ox}}{\varepsilon_S}\sqrt{\frac{q_b 2C_S}{C_{ox}}}\,sign(\alpha)\sqrt{e^{\frac{\varphi_S - V}{\varphi_t}} - e^{\frac{\varphi_0 - V}{\varphi_t}} - \left(\frac{\varphi_S - \varphi_0}{\varphi_t}\right)}, \tag{2}$$

where $\varepsilon_s$ is the silicon dielectric constant; $\varepsilon_{ox}$ is the $SiO_2$ dielectric constant; $t_{ox}$ is the equivalent dielectric thickness, EOT; gate capacitance per unit of area is equal to $C_{ox} = \varepsilon_{ox}/t_{ox}$; the silicon layer capacitance per unit of area is equal to $C_s = \varepsilon_s/t_S$ and $\varphi_o$ is the potential at the center of the layer. $q_b$ is the total fixed charge in the silicon layer $Q_b$, normalized to $C_{ox}\varphi_t$, with $\varphi_t$ being the thermal potential:

$$q_b = \frac{qN_D t_S}{C_{ox}\varphi_t} = \frac{Q_b}{C_{ox}\varphi_t} \tag{3}$$

In the calculations, it is convenient to normalize to thermal potential, $\varphi_t$, the value of the difference of potentials between the surface and the center of the silicon layer, which will be defined as:

$$\alpha = \frac{\varphi_S - \varphi_0}{\varphi_t}. \tag{4}$$

At deep subthreshold regime, when full depletion is achieved, this magnitude can be expressed as [13]:

$$\alpha_{bt} = -\frac{Q_b}{8C_S\varphi_t} = -\frac{q_b C_{ox}}{8C_S}. \tag{5}$$

As already mentioned JLT can operate in two well defined operation modes or regions. Region 1 corresponds to the depletion mode and is achieved when: (i) the applied gate voltage $V_G$ is lower than the flat band voltage plus the applied voltage $V$ at a defined point between source and drain, $V_G < V_{FB} + V$, and (ii) the surface potential is lower that the potential at center, that is $\alpha < 0$. Region 2 corresponds to the accumulation mode when $V_G > V_{FB} + V$ and $\alpha > 0$. In the transition between both regions, the surface electric field and total charge change their signs. For this reason, the symbol of the *sign* is included in (2). In the final expressions the transition voltage is defined by $V = V_D$.

The surface potential as function of the potential at the center can be calculated with a very good approximation using the finite-difference method as [8]:

$$\varphi_S = \varphi_0 - \varphi_t\,\alpha_{bt}\left(e^{\frac{\varphi_0 - V}{\varphi_t}} - 1\right). \tag{6}$$

Substituting (4) and (5) in (6) and after some mathematical manipulation the difference of potential can be calculated by the following expression:

$$\alpha = \alpha_{bt} + LW\left[-\alpha_{bt}e^{-\alpha_{bt}}e^{\frac{\varphi_S - V}{\varphi_t}}\right], \tag{7}$$

where $LW$ is the Lambert function. This approximate determination of difference of potentials between surface and center shows good coincidences between simulated and calculated potentials, see Fig. 2.

The relation between the applied gate voltage, the voltage drop across the MOS structure, $V$, and the surface potential is given by:

$$V_G - V_{FB} = \varphi_S + sign(\alpha)\,\varphi_t\beta\sqrt{e^{\frac{\varphi_S - V}{\varphi_t}} - \xi\cdot\alpha - 1}, \tag{8}$$

where $\beta = \sqrt{\frac{q_b 2C_S}{C_{ox}}}$ and $\xi = \left(1 - \frac{1}{\alpha_{bt}}\right)$.

The exact solution of this transcendental equation for $\varphi_S(V_G, V)$ and $\alpha(V_G, V)$ can be obtained only numerically, however using an iterative method of third order this equation can be solved with only few iterations with a precision better that 1 mV.

The function to be calculated iteratively is:

$$f(x) = x + sign(\alpha(x))\,\beta\sqrt{e^x - \xi\cdot\alpha(x) - 1} - \left(\frac{V_G - V_{FB} - V_D}{\varphi_t}\right), \tag{9}$$

where

$$x = (\varphi_S - V_D)/\varphi_t \text{ and} \tag{10}$$

$$\alpha(x) = \alpha_{bt} + LW[-\alpha_{bt}e^{-\alpha_{bt}}e^x]. \tag{11}$$

After the derivatives $f_n(x) = \frac{\partial^n f}{\partial x^n}$ are calculated, function $g(x)$ is calculated as:

$$g(x) = -\frac{f(x)}{f_1(x)}\left[1 + \frac{f(x)\cdot f_2(x)}{2f_1(x)^2} + \frac{f(x)^2}{6f_1(x)^4}\left(3f_2(x)^2 - f_1(x)\cdot f_3(x)\right)\right]. \tag{12}$$

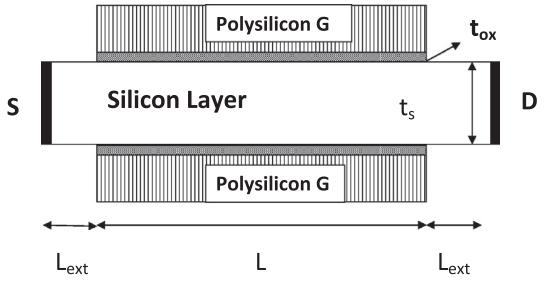


**Fig. 1.** Junctionless double-gate transistor structure.

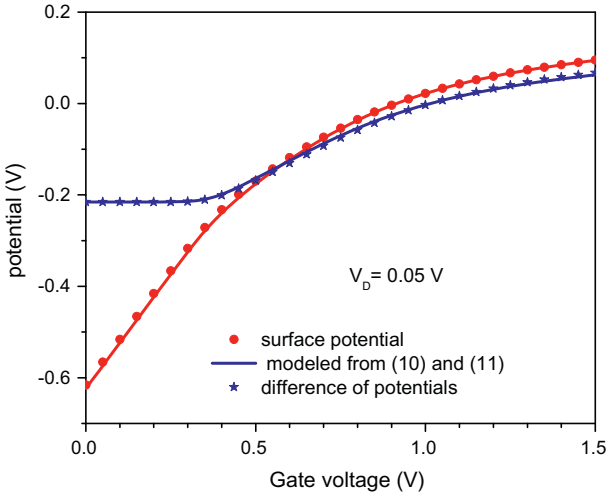


**Fig. 2.** Comparison of surface potential and difference of potentials surface-center between simulated data and calculated by (10) and (11) at $V_D = 50$ mV, $N_D = 5 \times 10^{18}$ cm$^{-3}$, $t_S = 15$ nm.