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Novel Si–Ge–C superlattices and their applications

Carlos J.R.P. Augusto *, Lynn Forester

Quantum Semiconductor LLC, 4320 Stevens Creek Blvd., Suite 212, San Jose, CA 95129, United States

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ABSTRACT

This paper presents Si–Ge–C superlattices (SLs) strained to Si that have direct band-gaps across a wide range of energies in the Infra-Red, dipole matrix elements larger than 1E−3, and oscillator strengths larger than 1E−1. Due to their constituents, these SLs will be able to be monolithically integrated with CMOS, thereby enabling efficient light emission and light absorption devices such as Light Emitting Diodes (LEDs), LASERs, and Photo-Diodes, in close proximity to CMOS devices. Key applications include Silicon Photonics, Multispectral CMOS Image Sensors, and Wide Spectrum PhotoVoltaic Cells, among others.

1. Introduction

The development of efficient optical devices with Si-based technologies, suitable for monolithic integration with CMOS has been a goal for several decades. In order to achieve efficient light absorption and emission, it is necessary to have a direct band-gap and sufficiently large oscillator strengths. This is a general statement, regardless of the wavelength. For photonic circuitry and optical communications it is very desirable to have band-gap energies around 0.8 eV ($\lambda = 1.55$ μm) and smaller. For image sensing the entire Infra-Red (IR) range, from Short-Wavelength Infra-Red (SWIR), to Mid-Wavelength Infra-Red (MWIR) to Long-Wavelength Infra-Red (LWIR), is of high interest since different types of information can be extracted from the different wavelength ranges. With Multi-Junction PhotoVoltaic cells it is also very useful to be able to absorb photons in those IR regions, which are outside the range absorbed by Si and Ge, and which also enable to capture the "night glow" thereby generating electrical power during the night.

With CMOS technology approaching mesoscopic dimensions for the critical regions of MOSFETs [1], intra-chip and inter-chip optical interconnects have become key enablers to maintain the desirable trends captured by Moore's Law, and which were observable until recent CMOS generations. It is also important to note that the application of photonics for this purpose has requirements that differ considerably from those for conventional fiber optics communications [2].

Another major barrier to the desirable trends captured by Moore's Law, is the problem of power dissipation, which has led to the growing interest in Tunnel-MOSFETs, which offer a solution to this problem [3]. While the type of band offsets needed for Tunnel-NMOS can be obtained with SiGe random alloys strained to Si, the same is not true for the band offsets needed for Tunnel-PMOS. Also, it has been pointed out [4] that a key problem of Si and SiGe-based Tunnel-MOSFETs is the limited ON-state current due to the inefficiency of band-to-band tunneling processes inherent to indirect band-gap materials in which the top of the valence band (VB) and the bottom of the conduction band (CB) occur at different points of *k*-space.

Consequently, there are multiple important applications that can significantly benefit from monolithically integrated active regions with direct band-gaps and useful oscillator strengths. All this has led to the pursuit of several different approaches to achieving efficient light emission from Si-based devices, including: $(Si)_m$–$(Ge)_n$ SLs; defect engineering of states in the gap of Si; Er-doping of Si and/or SiO_2, epitaxial $FeSi_2$; tensile strained Ge; and GeSn alloys grown on Ge layers (often relaxed buffer layers grown on Si); and the integration of III/V materials with silicon.

Each of these approaches has different advantages and disadvantages, but most of them require the active regions to be epitaxially grown on buffer layers on Si substrates. In order to achieve lower defectivity levels, which are still typically larger than 1E6/cm^2, the buffer layers are usually more than 1 μm thick, which presents a major challenge for planarization, since for monolithic integration with contemporary, high-yielding, CMOS processes, the height of the MOSFETs is typically less than 200 nm.

Therefore it is very desirable to have alternative ways of achieving direct band-gaps having large oscillator strengths with materials and devices that can be pseudomorphically grown directly on a silicon active region, which is the case with the Si–Ge–C superlattices (SLs) described in the next sections.

* Corresponding author. Tel.: +1 408 243 2262.
E-mail address: Carlos.Augusto@Quantumsemi.com (C.J.R.P. Augusto).

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2. Background

2.1. Previous work on Si-based superlattices

Theoretical modeling of the $(Si)_m$–$(Ge)_n$ SLs [5], where "m" and "n" are, respectively, the number of atomic planes for Si and Ge, established that for SL crystals grown along the <100> direction, a direct band-gap could be obtained through zone folding of the $2\Delta_{\perp}$-valleys perpendicular to the substrate surface plane (i.e., parallel to the SL axis), if these were lowered (in energy) with respect to the in-plane 4Δ// -valleys, as shown in Fig. 1. For SLs made using only Si and Ge, this configuration could not be achieved with films grown pseudomorphically on Si, but could be achieved by placing Si layers under tensile strain [6], i.e., performing the epitaxial growth of the SL on a $Si_{1-x}Ge_x$ relaxed buffer, which would have the added benefit of allowing at least partial strain compensation. The already mentioned high defectivity of SiGe buffer layers was the likely reason for the previous absence of good $(Si)_m$–$(Ge)_n$ photo-diodes, LEDs, or LASERs, using this approach. However, recently Ge-based layers/devices, tensile strained to relaxed Ge buffer layers, have demonstrated lasing action [7].

Nonetheless, theoretical work on this type of SL continues, and SL compositions arrived at with genetic algorithms indicate that oscillator strengths larger than 1E−2 are possible [8].

The previous work on $(Si)_m$–$(Ge)_n$ SLs was performed almost exclusively on SLs grown on crystalline (100) surfaces. However, the CB of Si and CB of Ge have energy minima, respectively, along the *X*-direction and the *L*-directions of the Brillouin Zone (BZ). Different surface orientations lead to different alignments between the direction of strain and the directions of symmetry in the BZ. Consequently, the SL-constituent materials and the SLs can have very different band structures depending on the surface orientation on which the pseudomorphic growth takes place. The possibility of having silicon wafers with multiple sets of active areas, each with different crystalline orientation [9,10], enables the utilization of surface orientation as a tool for band structure engineering. However, there is much less experience in the epitaxial pseudomorphic growth of heterostructures on (110) or (111) surfaces than on (100) surfaces, which could delay the availability of high-quality SL layers on these surfaces.

2.2. Si–Ge–C superlattices

The splitting in the CB of Si can also be produced through the incorporation of carbon into the Si layers [11], i.e., with $Si_{1-y}C_y$ films strained to Si, as shown in Fig. 2.

Therefore, by taking $(Si)_m$–$(Ge)_n$ SLs and replacing the pure Si layers with $(Si_{1-y}C_y)$ alloys, the theoretical condition required for SLs with direct band-gaps is achieved with films pseudomorphic

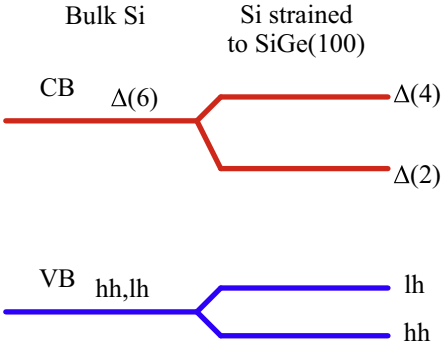

Fig. 1. Impact on the band edges of placing Si under tensile strain [see Ref. [6]].

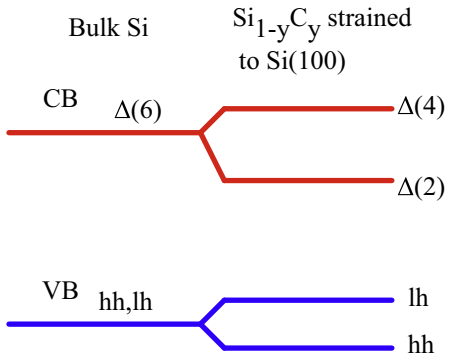

Fig. 2. Impact on the band edges from inserting C into the Si lattice ($Si_{1-y}C_y$ alloys) Ref. [11].

to the Si lattice constant. SLs strained to Si, of the form $(Si_{1-y}C_y)_m$–$(Ge)_n$, shown in Fig. 3, or $(Si_{1-y}C_y)_m$–$(Si_{1-x}Ge_x)_n$, can be grown directly on the surface of a CMOS active area, with the possibility of partial strain compensation depending on the combination of the amount of C and SL periodicity.

A schematic band diagram of a $(Si_{1-y}C_y)_m$–$(Ge)_n$, with 7% substitutional carbon in shown in Fig. 4, in which "m" and "n" are the number of atomic planes for the $Si_{1-y}C_y$ alloy and Ge, respectively, and the band offsets are obtained by the empirical expressions [11]:

$$\Delta E_g = -y \cdot ((6.5 \pm 0.3)\ \text{eV}),$$
$$\Delta E_C(\Delta 2) = -y \cdot E(4.6\ \text{eV}),$$
$$\Delta E_V(\text{lh}) = -y \cdot (1.9\ \text{eV}).$$

Conventionally, epitaxial $Si_{1-y}C_y$ layers are random alloys with fully substitutional carbon content up to only a few percent, which in the case of layers grown by CVD is approximately 3.2% or less [12]. However, it was demonstrated by MBE growth that Si_4C (20% C) *ordered alloys* can be pseudomorphic on Si [13,14]. Theoretical studies [15] have analyzed the precursor molecules for CVD growth, the corresponding crystal structures, and the band structures for Si_4C, as well as other ordered alloys with high C content. The band structures were not calculated for films strained to Si, but rather for "bulk" materials, relaxed to their natural lattice constants, which would require substrates with suitable lattice constants, a problem without an obvious solution.

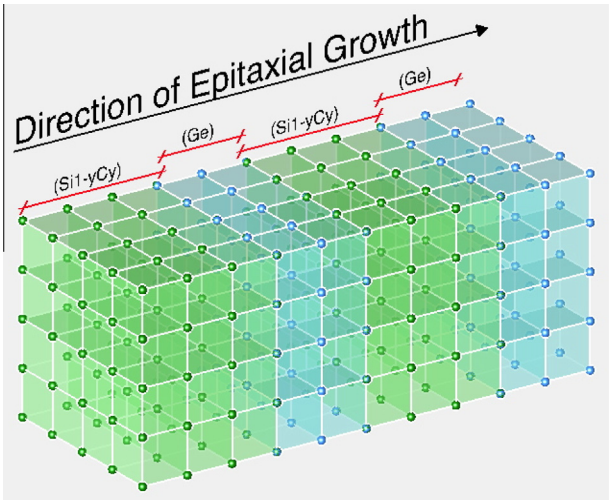

Fig. 3. Schematic of $(Si_{1-y}C_y)_m$–$(Ge)_n$ SLs.