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Fabrication and properties of GeSi and SiON layers for above-IC integrated optics

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ABSTRACT

A study is presented on silicon oxynitride material for waveguides and germanium–silicon alloys for p-i-n diodes. The materials are manufactured at low, CMOS-backend compatible temperatures, targeting the integration of optical functions on top of CMOS chips. Low-temperature germanium–silicon deposition, crystallization and doping are studied for integrated photo detection up to ~1500 nm wavelength. An investigation of the process window for laser crystallization is presented aiming toward the localization control of crystal boundaries and the achievement of crystals larger than 2 μm. Further, an inductively-coupled-plasma chemical vapor deposition process is presented for silicon oxynitride manufacturing at 150 °C wafer temperature, yielding low-loss material in a wide optical spectral range. Integration schemes for an optical plane on top of CMOS using these materials are discussed.

1. Introduction

The semiconductor industry is adjusting focus toward the so-called "More than Moore" innovation paradigm. By this is meant that microchip progress may not only follow from technology driven progress like miniaturization such as described by Moore [1], but can also come from the addition of new components and new functions inside the microchip. Examples are the introduction of passive components [2], biosensors [3], spin logic [4] and plasmonics [5], to name a few.

The fabrication sequence where the CMOS electronics is first fabricated (devices as well as multilevel interconnect), then followed by the subsequent fabrication of additional devices on top of this stack, draws particular interest, for its compactness, high performance potential and manufacturing convenience. This approach, dubbed Above-IC or CMOS post-processing, has been pursued since the 1980's [6]. It offers great opportunities for the field of microelectronics [7,8].

The monolithic integration of optical with electrical functions can already boast large commercial successes, such as digital micromirror technology [6] and CMOS active pixel sensors [9]. These examples are application-specific; to offer generic optical functionality in integrated circuits, a platform technology is required with the basic optical and electro-optical building blocks.

In this article we present investigations toward the integration of optical functions on top of CMOS, along the lines discussed in [10]. In particular, we pursue the monolithic integration of an optocoupler: a photonic data connection with electronic input and output (see e.g. [11]). An optocoupler consists of an electrically modulated light source, a light waveguide, and a photodetector. Integrated light sources are beyond the scope of the present article. In this paper, materials for light detection as well as waveguiding are studied, expanding on our earlier publications [12,13]. This article provides additional background information and presents new data to support the choices made in process optimization. We further present and compare integration schemes for these materials in the Above-IC context.

2. Process integration scenarios

The light source for integrated optical functions in microelectronics is normally an external (laser) light source [14], as an efficient integrated light source is not yet available in silicon technology. The CMOS substrate is opaque, so the obvious access routes for incoming light are from the side or from above the chip. For example, the integrated optical platform developed by Luxtera and ST [15] currently connects fibers from the top, but the third generation introduces side-connectivity to improve the form factor.

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For photodetection we envisage a p-i-n diode as argued e.g. in [16]. Three arrangements can couple waveguides to p-i-n photodetectors: in-plane, detector-first or waveguide-first, as sketched in Fig. 1. In the in-plane arrangement of Fig. 1a, the quality of the connecting interface between the two is a key point of concern. At this (vertical) interface, it is difficult to control the flatness, the composition and the interface quality when normal microfabrication techniques are used. Issues include the risk of lower-density materials formed during deposition over a step, contamination of the sidewall during anisotropic etching, process control of the etching angle and sidewall roughness. The presence of highly doped regions close to the waveguide should be avoided to prevent absorption of photons to be detected. This limits the possible configurations and particularly complicates the integration of vertical p-i-n stacks.

Detector-first (Fig. 1b) or waveguide-first (Fig. 1c) then seems a better choice, where the waveguide crosses the intrinsic part of a lateral p-i-n diode. The fabrication of a horizontal interface is generally much better controlled, and is easier modified, e.g. by polishing. As the electronics are at the bottom side and the light source comes from the side or the top, the detector-first arrangement (Fig. 1b) seems more convenient to interconnect. In this case, the upper layer of the detector is where most of the photoconversion takes place. This seems an appropriate choice in particular for polycrystalline semiconductor layers, as these commonly have larger crystals and less defects at the upper side, whereas the bottom interface can be rather difficult to control. As an intermediate solution between Fig. 1a and c, the detector can be fabricated to wrap around the waveguide (see e.g. [17]).

A general consideration in these arrangements is the absorption length of the chosen wavelength in the semiconductor, which determines the geometrical parameters (layer thickness, lateral size). Similarly the dimensions of the waveguide determine the optical modes as well as the confinement of the electromagnetic energy (related to losses). As they critically determine the system performance, ideally, the dimensions of the waveguide and the photodetector are separately optimized. When multiple wavelengths occur in the system (e.g. WDMA), different lateral sizes may be designed to accommodate these.

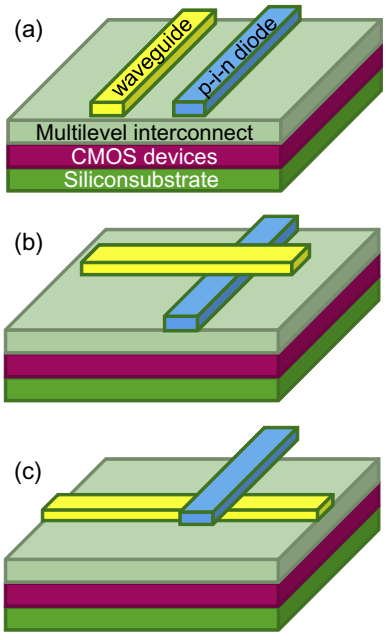

Fig. 1. Three arrangements for the integration of waveguides and photodetectors on top of CMOS. (a) in-plane positioning; (b) detector-first arrangement; (c) waveguide-first arrangement.

3. Polycrystalline germanium silicon

Silicon is an excellent material for photodetection in the visible range, as exemplified by the success of CMOS active pixel sensor imagers [9]. Above-IC formation of silicon photodiodes was successfully achieved about a decade ago [18,19]. However, silicon becomes transparent in the near-infrared. Germanium detectors are therefore studied as an alternative (see e.g. [17]). Finer tuning of the responsivity is possible using germanium–silicon alloys. This is illustrated by Fig. 2, which presents the responsivity of a simple p-i-n diode in Si_xGe_{1-x} alloys as a function of the silicon fraction x. These films are conveniently deposited using low pressure chemical vapor deposition (LPCVD) at CMOS back-end compatible temperatures. Our work focused on the optimization of GeSi alloys with $x = 0.85$ but the results can be generalized to a broader range of germanium–silicon ratios.

P-i-n diodes can either be formed by sequential deposition of in-situ doped layers, or by the deposition of an undoped layer followed by local formation and activation of highly doped n and p regions. In the above-CMOS integration scheme a vertical p-i-n diode seems less convenient, as discussed in section 2. Therefore, we consider the formation of lateral p-i-n structures necessary, and as a result local doping and activation must be pursued.

Given the tight thermal budget constraint in above-IC manufacturing, a furnace or rapid thermal anneal is too hot for the activation of p-type and n-type regions at appreciable doping levels. Therefore pulsed-laser crystallization is employed here to briefly reach a very high local temperature in the GeSi alloy without too much heating of the substrate underneath. By enforcing superlateral grain growth [20,21], sketched in Fig. 3, laser crystallization leads to very large crystal grains with a preferred orientation.

Grain boundaries in the polycrystalline material lead to reduced conductivity and component variability. To steer the grain location during the crystallization process, a periodic lateral thickness variation was formed orthogonal to the laser scan direction using a GeSi line pattern covered by a blanket GeSi layer. The laser treatment is optimized for sequential super-lateral growth to occur only in between the patterned lines.

The process window was determined by systematically varying the process parameters (laser beam width, pulse energy, pulse overlap) and physical analysis of the samples, mostly by scanning

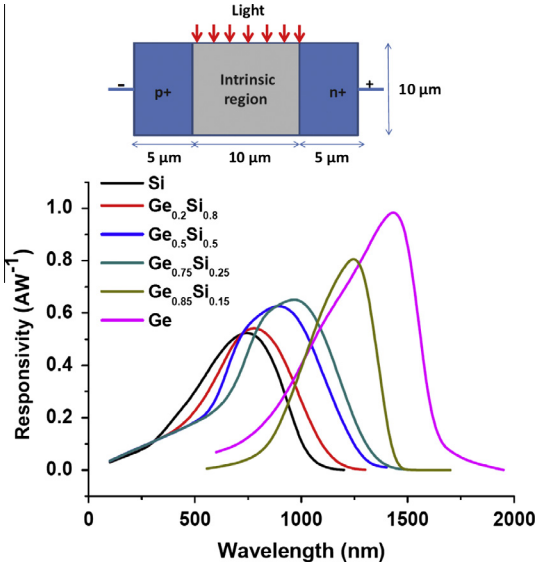

Fig. 2. Room-temperature responsivity of p-i-n photodiodes in monocrystalline germanium–silicon alloy, depending on wavelength and alloy composition, simulated by Silvaco-Atlas (the simulated geometry is depicted in the upper sketch).