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Large scale integration of graphene transistors for potential applications in the back end of the line

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ABSTRACT

A chip to wafer scale, CMOS compatible method of graphene device fabrication has been established, which can be integrated into the back end of the line (BEOL) of conventional semiconductor process flows. In this paper, we present experimental results of graphene field effect transistors (GFETs) which were fabricated using this wafer scalable method. The carrier mobilities in these transistors reach up to several hundred $cm^2 V^{-1} s^{-1}$. Further, these devices exhibit current saturation regions similar to graphene devices fabricated using mechanical exfoliation. The overall performance of the GFETs can not yet compete with record values reported for devices based on mechanically exfoliated material. Nevertheless, this large scale approach is an important step towards reliability and variability studies as well as optimization of device aspects such as electrical contacts and dielectric interfaces with statistically relevant numbers of devices. It is also an important milestone towards introducing graphene into wafer scale process lines.

1. Introduction

In today's semiconductor technology, there is a growing trend to not only scale devices and increase their density on a wafer (more Moore), but also to increase the functionality of integrated circuits as a whole (more than Moore). Devices integrated on chip are no longer relegated to performing logic operations or memory functions, but may provide electronic and electromechanic sensing for environmental feedback or radio frequency (RF) analog data handling for high speed wireless communication. Research into graphene has progressed rapidly – and a number of potential more than Moore applications are being investigated from sensors [1,2] to radio frequency (RF) devices [3–5] and photodetectors [6,7]. Graphene can have high carrier mobility on SiO_2 substrates (up to 20,000 $cm^2 V^{-1} s^{-1}$) [8] and shows high velocity saturation [9]. Clear current saturation and high transconductance have also been measured for large area devices fabricated using pristine (mechanically exfoliated) graphene [10]. These extraordinary electronic properties have fueled research into graphene field effect transistors (GFETs) [11], in particular for RF applications. This is due to the absence of an electronic band gap, which leads to poor on to off current ratios (I_{on}/I_{off}) in GFETs and limits their use in conventional digital circuits [12]. In RF devices, in contrast, switching with high I_{on}/I_{off} ratios is a less stringent requirement [3,13,14]. At present, several experimental demonstrations of simple GFET-based circuits are available [15–19], as well as device models that enable further exploitation in circuit design [10,20–23].

One of the most crucial steps towards commercializing graphene devices and circuits, besides demonstrating prototypes in experiments, is to establish wafer scale processes that are compatible with existing process technology. In this work, we show the feasibility of a large scale graphene process flow for fabrication of GFETs. This fabrication method can be implemented in the back end of the line (BEOL) of a CMOS compatible process, is in principal scalable to any wafer size, and could potentially allow for the integration of RF transistors and circuits or other graphene-based devices in system on chip (SoC) applications, adding system functionality.

2. Experimental

Fig. 1a shows a schematic of the GFET fabrication process, which in detail comprises of the following steps: Devices are fabricated using a silicon substrate covered with a 1.8 μm layer of thermally grown silicon dioxide (SiO_2) (Fig. 1a-1). Reactive ion etching

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(RIE) is used in order to selectively etch through the SiO_2 layer to form electrical contacts to the substrate (Fig. 1a-2). The RIE process uses 200 mW power at 40 mTorr. Aluminum is then deposited using e-beam evaporation into the contact holes in order to act as vias to the substrate/back gate. The aluminum via is patterned using standard photolithography and lift-off (Fig. 1a-3). RIE is similarly used to etch 640 nm deep trenches into the SiO_2 layer, which are then filled with an adhesion layer of 160 nm of titanium followed by 500 nm of gold to form drain and source contacts (Fig. 1a-4). Evaporation into the trenches effectively embeds the contacts in the SiO_2 layer, which allows the graphene to be transferred over the top of the contacts instead of forming the contacts on top of graphene. Embedding contacts before graphene transfer reduces the number of process steps after graphene is transferred, which reduces damage to the graphene layer. The drain and source contacts are patterned using lift-off. Note that the gold contacts can be replaced easily with suitable CMOS compatible metals and the lift-off process can be replaced with standard BEOL damascene technology. Graphene is then transferred to the wafer as shown in Fig. 1a-5. Commercially available 60 mm by 40 mm chemical vapor deposited (CVD) graphene from Graphenea is used for the transfer (http://www.graphenea.com/). Fig. 1b shows a graphical illustration of a 60 mm by 40 mm graphene patch transferred onto a 4″ wafer. Note that the graphene transfer process is limited by the available graphene size, not by the transfer method. The graphene transfer process is as follows: first, a layer of poly(Bisphenol A) carbonate (PC) is spin coated onto the copper and graphene in a common wet transfer method [24–28] as shown in Fig. 1b-1. Carbon residue is subsequently etched away from the back side of the copper using O_2 plasma. The copper/graphene/PC stack is then placed into ferric chloride in order to etch away the copper layer. This leaves a remaining graphene/PC stack floating in the etchant. The stack is then transferred to de-ionized (DI) water and 8% hydrochloric acid HCl in order to clean away remaining residues. It is then transferred to the destination wafer (Fig. 1b-2). The wafer is then baked at 45 °C on a hotplate for 10 min in order to evaporate remaining water as well as improve the adhesion between the substrate and the graphene. Acetone is used for initial cleaning of the wafer before placing it into chloroform overnight to etch the polymer layer (Fig. 1b-3). The graphene is then patterned using standard photolithography and etched using O_2 plasma (Fig. 1a-6). Metal evaporation is then used to deposit a 3 nm layer of aluminum onto the surface of the wafer. This layer is oxidized to act as a seed layer for subsequent deposition of 20 nm of Al_2O_3 using atomic layer deposition (ALD), leading to a 25 nm thick dielectric layer (Fig. 1a-7). The Al_2O_3 in areas of the wafer such as the contact pads are then selectively etched using photolithography and a wet chemical etchant (CD 26). A gate electrode is then deposited on top of the Al_2O_3 which consists of 50 nm of Ti and 150 nm of Au. Metal evaporation and lift-off are again used for the top gate (Fig. 1a-8). Finally, the chips are wire bonded and packaged for further experiments. Fig. 2a shows a color enhanced scanning electron microscope (SEM) image of a wire bonded GFET device. Wire bonds are shaded orange, drain and source contacts are shaded gold, the top gate is shaded yellow, the back gate is shaded blue, and the graphene channel is shaded light blue. Fig. 2b shows a wire bonded chip inside a 24 lead dual-in-line package (DiP).

3. Results and discussion

A schematic of the fabricated GFETs is shown in Fig 2c. A bias voltage can be applied to the device using the Ti/Au drain and source contacts (1). The graphene layer forms the transistor channel between source and drain (2). The devices also provide a contact pad for the Ti/Au top gate electrode (3), which is electrically isolated from the channel by a 25 nm Al_2O_3 layer (5). A 1.8 μm thick SiO_2 layer (6) separates the graphene channel from a silicon substrate, which can be used as a global back gate (7), with an Al via providing a contact pad for electrical probing (4).

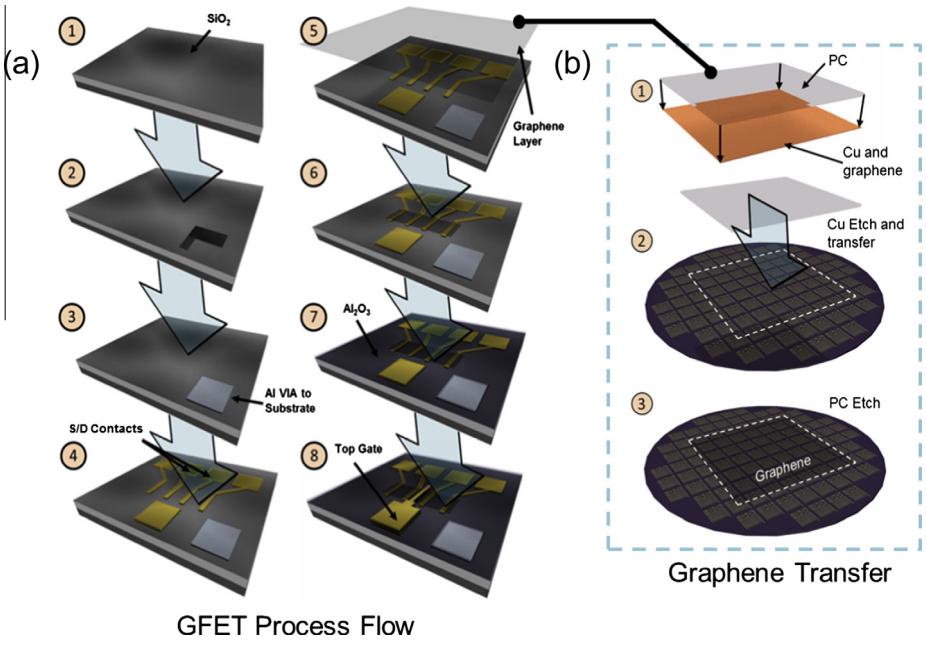

Fig. 1. (a) Schematic of the GFET process flow including the following process steps: thermal oxidation of silicon to form SiO_2 (1) via etching into the SiO_2 layer to the substrate using RIE (2) filling of the via with aluminum to act as a contact pad to the substrate (3) metal contacts patterning (4) graphene transfer (5) graphene patterning using O_2 plasma (6) Al_2O_3 gate oxide deposition on graphene (7) top gate formation (8) (b) graphical illustration of wafer scale transfer process using a 60 mm by 40 mm graphene sheet. Polycarbonate (PC) spin coating on Cu foil containing graphene (1) $FeCl_3$ etching of the Cu foil and transfer of the graphene/PC stack onto the wafer (2) etching of the PC layer in chloroform, leaving the graphene sheet on the wafer.