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The impact of interface states on the mobility and drive current of $In_{0.53}Ga_{0.47}As$ semiconductor n-MOSFETs

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ABSTRACT

Accurate Schrödinger-Poisson and Multi-Subband Monte Carlo simulations are used to investigate the effect of interface states at the channel-insulator interface of $In_{0.53}Ga_{0.47}As$ MOSFETs. Acceptor states with energy inside the conduction band of the semiconductor can explain the dramatic Fermi level pinning observed in the experiments. Our results show that these states significantly impact the electrical mobility measurements but they appear to have a limited influence on the static current drive of short channel devices.

1. Introduction

The replacement of silicon with III–V compound semiconductors as channel material in advanced MOSFETs has been widely investigated over the last years [1,2]. The surface trap-state density of III–V compounds is much larger than that of state of the art silicon/SiO_2 interfaces [3,4], and Hall mobility measurements have shown that the charging of these states results in a remarkable Fermi level pinning which precludes attaining a free carrier density larger than $N_S \approx 5 \cdot 10^{12}$ cm^{-2} [5,6]. This large trapped charge affects the electrostatics but it does not contribute to the drain current. Consequently, one of the basic assumptions at the foundation of split-CV mobility extraction techniques is violated [7].

In this paper, a self-consistent solution of the Schrödinger and Poisson equations in the presence of interface charge is used to extract the energy profile $D_{it}(E)$ of interface states. The extracted charge is then introduced in a Multi-Subband Monte Carlo (MSMC) simulator [8,9], both as a source of Coulomb scattering and as a contribution to device electrostatics, to asses its effect on low field electrical mobility and on the drive current, I_{ON}, of short channel devices.

The paper extends our previous report in [10] by providing a more detailed analysis of the experiments including Hall and electrical mobility.

2. Model description

Interface states have been introduced in the equilibrium solution of the coupled Schrödinger and Poisson equations as a sheet of charge at the interface between the channel and the gate dielectric. The Schrödinger equation is solved using the parabolic effective mass approximation, then the non-parabolicity correction from [11] is applied. If we let $E^P_{v,n}$ be the parabolic n-th subband minimum of valley v, then the corresponding non-parabolic subband minimum $E^{NP}_{v,n}$ is given by:

$$E^{NP}_{v,n} = U_{v,n} + \frac{\sqrt{1 + 4\alpha_v \cdot (E^P_{v,n} - U_{v,n})} - 1}{2\alpha_v}$$
$$U_{v,n} = \int |\xi_{v,n}(y)|^2 U(y) dy \quad (1)$$

where $U(y)$ is the confining potential along the quantization direction y, α_v is the non-parabolicity coefficient and $\xi_{v,n}$ is the wavefunction obtained with parabolic bands.

The model is thus appropriate for near equilibrium conditions to investigate, for instance, MOSFETs biased at low V_{DS} and low-field mobility measurements. The solution of the Schrödinger equation considers wave-function penetration in the dielectrics, which can be relevant in III–V materials [9],

The interface charge per unit area $Q_{it} = -qN_{it}$ is computed under the following assumptions: (a) traps below the semiconductor mid-gap (E_m) are donor-like, i.e., they contribute with a positive

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charge when empty [7]; (b) traps above the mid-gap are acceptor-like, i.e., they contribute with a negative charge when occupied by an electron [7]; and (c) the occupation probability $f(E, E_F)$ follows the equilibrium Fermi–Dirac statistics. We further choose to express D_{it} as:

$$D_{it}(E) = D_{it}(E_C) \cdot \left(10^{\sum_{i=1}^{n} a_i (E-E_C)^i}\right) \quad (2)$$

where E is the state energy. The N_{it} is then given by:

$$N_{it} = -\int_{-\infty}^{E_m} D_{it}(E) \cdot [1 - f(E, E_F)]dE + \int_{E_m}^{\infty} D_{it}(E) \cdot f(E, E_F)dE \quad (3)$$

where E_F is the equilibrium Fermi level and E_m is the energy level that separates donor-like from acceptor-like traps. Eq. (2) is polynomial on a semi-logarithmic scale. The shape of the D_{it} energy distribution is set by the coefficients a_i. $D_{it}(E_C)$ is the trap concentration at the conduction band edge (E_C) of the semiconductor in units of $eV^{-1}\,cm^{-2}$.

A correct choice of the $D_{it}(E_C)$, the polynomial degree, n, and coefficients, a_i, is necessary to reproduce experimental N_S and mobility curves [6,5]. Fig. 1 compares simulated $N_S(V_{GS})$ curves with experimental data from [6]. Polynomials of different degree can be used to fit the measurements but, after choosing the appropriate coefficients, the trap distributions are very similar as can be seen by looking at the D_{it} energy profiles in the inset. In the following, we have opted for the lowest degree $n = 2$ that results in a good agreement with the experiments. Also, this choice makes easier the task of finding the optimal coefficients.

To this end, we note that for the sole purpose of finding the best coefficients in Eq. (2), traps do not necessarily need to enter the coupled Schrödinger-Poisson problem explicitly; in fact, since wave-function penetration beyond the surface charge layer is modest, self-consistent calculations with traps can be accurately reproduced if the abscissa of a simulated $N_S(V_{GS})$ curve without traps is "stretched" by an amount equal to $-Q_{it}(V_G)/C_{OX}$. Fig. 2 illustrates the use of this technique. The stretching implies that the same N_S is found at a higher gate voltage in the case with traps.

To extract the D_{it} energy spectrum and determine the fitting parameter values we set up a global optimisation problem whose solution is the set of a_i and $D_{it}(E_C)$ coefficients that yields the best agreement between measured and simulated $N_S(V_{GS})$ curves. In other words, we have to find the correction term $Q_{it}(V_{Gsim})$ that minimises the difference between the experimental and simulated $N_S(V_{GS})$. In formula, the problem is to minimise:

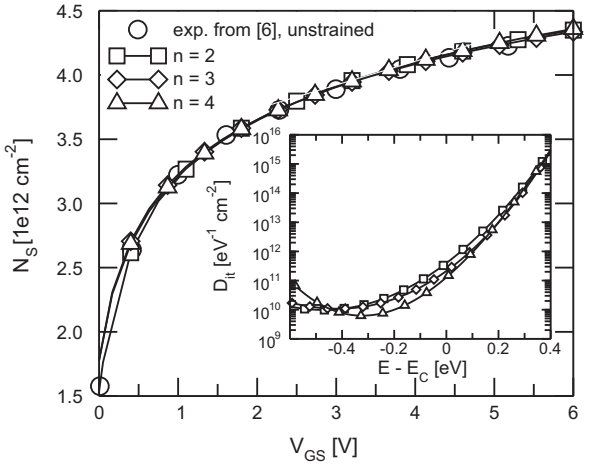

Fig. 1. Simulated $N_S(V_{GS})$ for different polynomial degree n in Eq. (2). The inset shows the extracted D_{it} corresponding to each polynomial function.

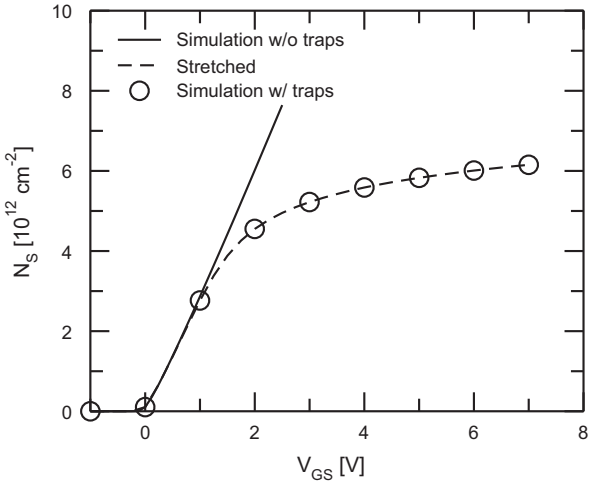

Fig. 2. Illustration of the stretching technique used to fit the free carrier density versus gate bias curves. First, an $N_S(V_{GS})$ curve is simulated without considering the effect of interface traps (solid line); then, this curve is stretched by $-Q_{it}(V_{GS})/C_{OX}$ (dashed line). The circles represent $N_S(V_{GS})$ simulations with the full self-consistent loop considering the effect of interface traps. The agreement between the dashed curve and the symbols proves the validity of the proposed extraction algorithm.

$$\left\| V_{Gexp}(N_{Sexp}) - \left(V_{Gsim}(N_{Ssim}) - \frac{Q_{it}(V_{Gsim})}{C_{OX}}\right)\right\|_2^2 \quad (4)$$

where $V_{Gsim}(N_{Ssim})$ is obtained from simulations without interface traps. The search for the solution of the minimisation problem (that is, the sought set of $D_{it}(E_C)$ and $a_1, \ldots, a_n$) must be adequately constrained, otherwise the result may still fit the experiments but with an unrealistic D_{it} profile. In particular, based on results in [5], we expect D_{it} profiles with exactly one minimum at a specific energy (e.g. the midgap) and no maximum. It is not always straightforward to satisfy these requirements, but if the polynomial is a second order one, we just need to enforce a_2 to be positive. Note that, since the D_{it} is fitted on Fermi level pinning experiments, it may end up being inaccurate in the gap. We will return later on this point.

Note that the stretching technique described so far is used only for the purpose of finding the optimal coefficients of Eq. (2), whereas in the other calculation of this paper, the full self-consistent problem is solved.

3. Results: Fermi level pinning and D_{it} profiles

We define the Fermi level pinning as the condition at which an increase of the gate voltage corresponds to a very small increase of the Fermi level with respect to the minimum of the conduction band, and we consider MOSFETs at equilibrium ($V_{DS} = 0$ V), consistently with the bias used during Hall mobility measurements and $N_S(V_{GS})$ extraction. Fig. 3 reports a few of the $N_S(V_{GS})$ as measured by different groups [5,6,12]. The curves saturate at high gate voltage, indicating Fermi level pinning. If we express D_{it} as in Eq. (2) and determine the coefficients $D_{it}(E_C), a_1$ and a_2 by solving the minimisation problem of Eq. (4), good agreement between our model and experiments can be obtained.

Each data set saturates at a different free carrier density, therefore in principle each set has a different D_{it} profile. Fig. 4 reports the $D_{it}(E)$ over the energy range spanned by the Fermi level when V_{GS} spans from approximately 0V to the maximum V_{GS} in the experiments (see Fig. 3). Interestingly, the spread between the various D_{it} profiles is not too large for the considered $In_{0.53}Ga_{0.47}As/Al_2O_3$ devices, demonstrating a comparable degree of maturity in the fabrication process. However, given the exponential increase of $D_{it}(E)$, small horizontal shifts of energy have