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Capacitance estimation for InAs Tunnel FETs by means of full-quantum $\mathbf{k}\cdot\mathbf{p}$ simulation

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ABSTRACT

We report for the first time a quantum mechanical simulation study of gate capacitance components in aggressively scaled InAs Nanowire Tunnel Field-Effect Transistors. It will be shown that the gate-drain capacitance exhibits the same functional dependence over the whole V_{gs} range as the total gate capacitance, albeit with smaller values. However, as opposed to the previous capacitance estimations provided by semiclassical TCAD tools, we find that the gate capacitance exhibits a non-monotonic behavior vs. gate voltage, with plateaus and bumps related with energy quantization and subband formation determined by the device cross-sectional size, as well as with the position of channel-conduction subbands relative to the Fermi level in the drain contact. From this point of view, semiclassical TCAD tools seem to be inaccurate for capacitance estimation in aggressively-scaled TFET devices.

1. Introduction

Novel device concepts are being widely studied to overcome scaling limitations of traditional planar bulk CMOS technologies, such as short-channel effects and leakage currents. One major issue with conventional MOSFETs is that carrier injection at the MOSFET source-channel junction is bound by the exponential tail of Fermi statistics because it is governed by thermionic emission over a potential barrier [1]. This implies that the MOSFET inverse subthreshold slope (SS) cannot be reduced below 60 mV/decade at room temperature [2]. However, power-dissipation increase in next-generation digital systems must be contrasted by reducing the voltage supply V_{DD}. To this purpose, transistors with SS $\simeq$ 45 mV/decade or lower, on at least three decades of drain current I_{ds}, should be designed [3].

A possible candidate to replace conventional CMOS is the Tunnel FET (TFET) [4,5], which is expected to provide very steep subthreshold slopes and, thus, reduced supply voltages, while retaining full compatibility with CMOS technology. The TFET structural similarity with standard MOSFETs makes it possible to take advantage from the evolution of CMOS technology, allowing for both horizontal and vertical implementations with double-gate (DG) and gate-all-around (GAA) configurations. Besides, the use of intrinsic channels promises reduced random-dopant induced variability. Current challenges to mainstream introduction of the TFET technology include the difficulty to achieve sufficiently high on-state currents. However, merely increasing I_{on} does not necessarily result in a better TFET-based circuit performance [6].

Standard performance metrics for digital circuits are propagation delay and power dissipation. The device properties affecting the aforementioned parameters are the drive current in saturation and linear regions, the gate and Miller capacitances, and the output conductance. Hence, a detailed understanding of TFET capacitances is essential for the design of TFET-based circuits [7]. It was shown in [8] that the partitioning of the total gate capacitance C_{gg} in a TFET is significantly different from that in a MOSFET, fundamentally due to the difference in inversion charge distribution. For a MOSFET operating in the linear region, both source and drain (S/D) regions are connected to the channel, and C_{gg} is evenly split into source and drain contributions: $C_{gd} \simeq C_{gs} \simeq C_{gg}/2$, with C_{gs} the gate-source and C_{gd} the gate-drain capacitances, respectively. In saturation, $C_{gs} \simeq 2/3\, C_{gg}$, and $C_{gd} \simeq 0$. For a TFET, instead, the drain is connected to the channel both in linear and saturation regions. C_{gd} and C_{gs} are thus unequal, with C_{gd} representing a larger fraction of C_{gg}.

To our knowledge, the calculation of TFET parasitic capacitances has only been carried out with semiclassical TCAD tools so far [8]. The accuracy of such tools may be questionable when aggressively-scaled devices are investigated. In contrast with the majority of published papers, a full-band quantum simulation approach is used in this work to properly account for quantum effects, which strongly influence TFET devices, and the dependence of C_{gg}, C_{gd}

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and C_{gs} on terminal voltages and device size. The paper is organized as follows. The device structure and the simulation approach are illustrated in Section 2. Section 3 presents the total gate capacitance characteristics and discusses its trend with respect to quantum-mechanical effects. The partitioning of C_{gg} into C_{gd} and C_{gs} is investigated in Section 4. Finally, conclusion remarks are given in Section 6.

2. Analysis approach

The simulator employed for the present investigation is based on a four-band $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian [9] to accurately model multi-band effects and the complex band structure of our devices. All calculations are carried out in a fully 3-D framework, accounting for anisotropic effects. A nonequilibrium Green's function (NEGF) formalism [10] is employed for transport description within the ballistic approximation, which is expected to be a reasonable assumption for the gate lengths considered here due to the high mobility and, hence, long mean-free paths, of electrons in III–V materials. The NEGF module is self-consistently coupled with a 3-D Poisson solver for electrostatics computation.

Material parameters are taken from [11] and bowing effects are accounted for. Stress effects are not considered in this work. Contact resistances and parasitic capacitances are not addressed either, as their impact is strongly dependent on the actual device implementation, which is beyond the scope of this work.

The InAs homojunction n-TFET shown in Fig. 1 is addressed for this investigation. The device features 20 nm-long channel and S/D regions; Al_2O_3 gate dielectric with EOT = 1 nm is assumed; source and drain doping levels are set to $N_S = -5\times10^{19}$ cm^{-3} and $N_D = 5\times10^{19}$ cm^{-3}. Three different cross sectional areas have been investigated, with L_{side} = 3.4, 5 and 7 nm, respectively, in order to clarify the effect of quantum confinement on the capacitance behavior.

Capacitances are extracted by computing the change of the gate charge Q_g relative to a small change in terminal voltages at every bias conditions, namely:

$$C_{gg} = \left.\frac{\partial Q_g}{\partial V_g}\right|_{V_s,V_d} \quad C_{gd} = -\left.\frac{\partial Q_g}{\partial V_d}\right|_{V_s,V_g} \quad C_{gs} = -\left.\frac{\partial Q_g}{\partial V_s}\right|_{V_d,V_g}$$

More specifically, C_{gg} and C_{gd} are extracted at each bias point by evaluating the gate charge variation following a small gate or drain voltage variation ($\Delta V = 10$ mV), respectively. Then C_{gs} can be computed knowing that $C_{gs} + C_{gd} = C_{gg}$. In all simulations the source voltage is fixed at 0 V.

3. Gate capacitance characteristics

Drain currents computed for the three devices at $V_{ds} = 0.05$ V and 0.5 V are shown in Fig. 2. The current is normalized with respect to the side of the square cross-section. The larger cross-sections lead to a higher drain current, due both to the bandgap decrease that increases the band-to-band tunneling probability, and to the reduced subband splitting, that enables a larger population within the second and higher subbands. However, the smaller bandgap is responsible for the ambipolar effect, that shows up at low V_{gs} and high V_{ds}.

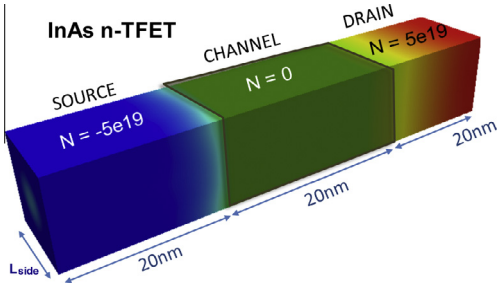

Fig. 1. Structure of the simulated n-type TFET, with indication of source, channel and drain lengths, as well as doping levels in cm^{-3}. Abrupt profiles are assumed. Al_2O_3 has been chosen as gate dielectric with EOT = 1 nm. The device cross-sections L_{side} vary from 3.4 to 7 nm.

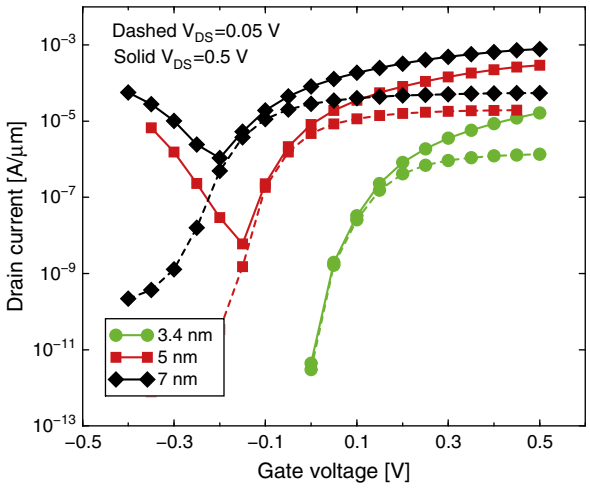

Fig. 2. Turn-on characteristics of the three nanowire TFETs with 7 × 7, 5 × 5 and 3.4 × 3.4 nm^2, computed at $V_{ds} = 0.05$ V (dashed lines) and 0.5 V (solid lines). The computation is carried out with an in-house, full quantum, four-band $\mathbf{k}\cdot\mathbf{p}$ simulator especially developed for the investigation of nanowire TFETs as that shown in Fig. 1.

The total gate capacitance C_{gg} computed at $V_{ds} = 0.05$ V (left) and 0.5 V (right) for the three devices is shown in Fig. 3. A $\Delta V_{gs} = 10$ mV is applied to compute C_{gg}. As previously shown in [7,8,12], the gate capacitance is largely reduced when the drain voltage is increased. However, our simulations predict a non-monotonic behavior of C_{gg} vs. V_{gs} at low V_{ds}, with bumps and plateaus at different gate voltages for the three cross sections. This is in contrast with results typically observed with semiclassical TCAD tools.

The gate capacitance of the smallest device ($L_{side} = 3.4$ nm) shows a maximum at $V_{gs} = 0.25$ V and then decreases. This effect

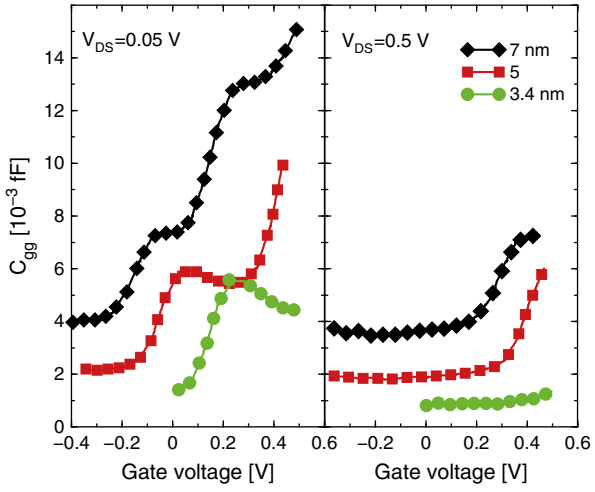

Fig. 3. Total gate capacitance C_{gg} of the three nanowire TFETs, computed at $V_{ds} = 0.05$ V (left) and 0.5 V (right). A $\Delta V_{gs} = 10$ mV has been applied to compute C_{gg}, which shows a non-monotonic behavior, with bumps and plateaus at different gate voltages for the three cross sections.