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AlGaN/GaN MOS-HEMTs-on-Si employing sputtered TaN-based electrodes and HfO_2 gate insulator

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ABSTRACT

We report on a low specific on-resistance ($R_{on,sp}$) of 3.58 mΩ-cm^2 and a high breakdown voltage of 1.4 kV in a CMOS-compatible AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistor (MOS-HEMT). The MOS-HEMT is on a Si substrate and uses TaN electrodes and a HfO_2-gate insulator. The sputtered TaN – a substitute for Au that has low resistivity, high work function, and thermal stability – was applied at room temperature to the gate, source, and drain. In order to obtain a low $R_{on,sp}$ and high breakdown voltage, sputtering power and post-annealing temperature were optimized by measuring the characteristics of TaN. Using optimized conditions, a sputtering power of 50 W, and an annealing temperature of 880 °C, we successfully achieved a high on/off current ratio of 6×10^9 for the proposed AlGaN/GaN MOS-HEMT at a gate–drain distance of 10 μm. These results indicate that the TaN process is a promising technique for power-switching GaN devices with CMOS compatibility.

1. Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) have proven their worth as next-generation high-power devices due to their wide bandgap properties such as high critical electric field, low intrinsic carrier concentration [1], and high-mobility channel that results from conduction-band discontinuity and polarization effects [2]. Compared to conventional semiconductor devices, AlGaN/GaN HEMTs have advantages for high-current and high-voltage operations. In addition, high-temperature operation of GaN-based power devices is very attractive for electric vehicle applications.

We know that a metal-oxide-semiconductor (MOS) gate is a suitable structure to suppress a gate leakage current, as well as any undesirable diode operation, through a Schottky gate in conventional HEMTs. We have already reported on high-quality RF-sputtered HfO_2 gate insulators in AlGaN/GaN MOS-HEMTs that have improved reverse blocking characteristics [3]. Systematic descriptions of various tests of the sputtered HfO_2 gate insulator successfully achieved a low specific on-resistance ($R_{on,sp}$) of 3.77 mΩ cm^2 and 1524 V in the AlGaN/GaN MOS-HEMT at a gate–drain distance (L_{GD}) of 20 μm [3].

Many research groups have reported on high-performance AlGaN/GaN MOS-HEMTs and GaN-on-Si growth technologies that reduce fabrication costs owing to their common and large-sized Si substrates. However, a CMOS-compatible process is required to compete against Si-based power devices. In addition, it has been well known that Au is not compatible with CMOS processes. For these reasons, the development of new electrodes that replace Au in compound devices has been considered a critical goal [4]. Multi-stacked Ti/Al/Ni/Au and Ni/Au have been widely used for basic structures in ohmic and Schottky contacts of AlGaN/GaN heterostructures, respectively [5]. Recently, Cu and W have been reported to replace the Au top layer of each electrode for CMOS compatibility [6,7]. Further investigation of substitute electrodes of Au is required because Cu is thermally unstable [8,9] and W is highly resistive. TaN is a promising candidate for electrodes without Au, owing to its excellent material properties such as low resistivity and highly thermal stability [10]. In the CMOS process, TaN has already been used as a thermal barrier layer under the Cu gate. Therefore, TaN is a suitable material for CMOS-compatible AlGaN/GaN devices [11]. Additionally, TaN gates for AlGaN/GaN MOS-HEMTs have been reported for their large work function of 4.5 eV [12–14].

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In this paper, we proposed TaN-gate and Ti/Al/TaN-ohmic contact AlGaN/GaN MOS-HEMTs with HfO_2 gate insulators for a CMOS-compatible process. In order to obtain a stable on/off current ratio and high breakdown voltage in the devices, the effects of sputtering conditions and annealing temperatures on electrical characteristics were investigated. As a result, we achieved a low $R_{on,sp}$ of 3.58 mΩ cm^2, high breakdown voltage of 1.4 kV, and high on/off current ratio of 6×10^9 at a L_{GD} of 10 μm. For comparison, conventional devices having Ni/Au gates and Ti/Al/Ni/Au ohmic contacts were also fabricated.

2. Device structure and fabrication

We used 200 mm GaN-on-Si (1 1 1) substrate grown by metal-organic chemical vapor deposition as a starting material. The structure was composed of the following layers: a 3.9-μm-thick C-doped GaN buffer, 100-nm-thick u-GaN buffer, 1-nm thick AlN spacer, 20-nm-thick u-$Al_{0.23}Ga_{0.77}N$ barrier, and 3-nm-thick u-GaN cap layers. First, we fabricated four types of conventional devices with the widely used Ti/Al/Ni/Au ohmic contact. The type-I device is a conventional HEMT with a Ni/Au gate. The type-II device is a conventional HEMT with a TaN gate. Type-III and IV devices are conventional MOS-HEMTs that have HfO_2 gate insulators. The gate electrode of type-III and IV devices are Ni/Au and TaN, respectively. The proposed device (type V) is a MOS-HEMT with a TaN gate and Ti/Al/TaN-ohmic contact, where TaN completely replaces Au. Cross-sectional views of the conventional devices (types I, II, and III) are shown in the supplemental data.

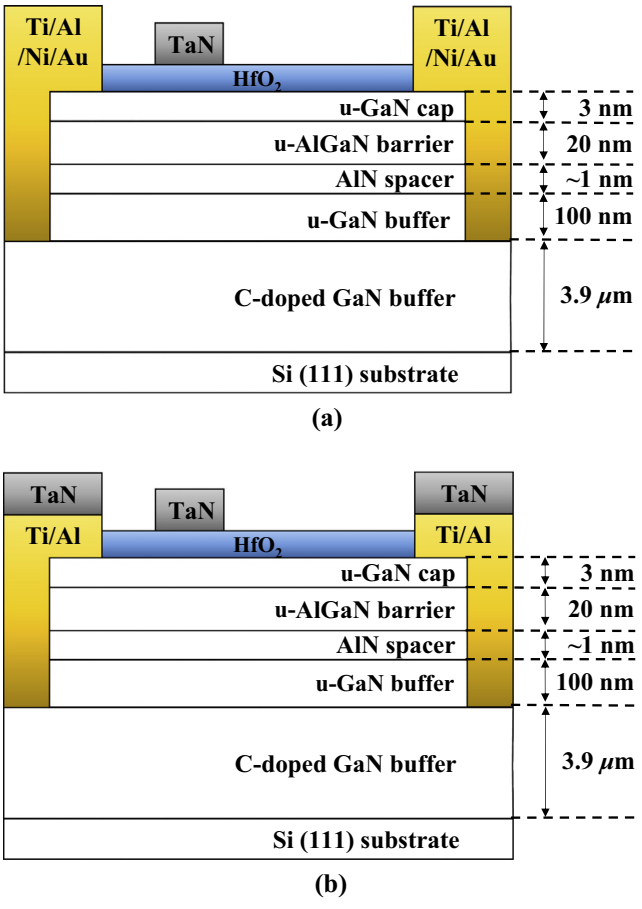

Fig. 1. Cross-sectional views of the conventional AlGaN/GaN MOS-HEMT with (a) Ti/Al/Ni/Au (type IV) and (b) Ti/Al/TaN (type V) ohmic contacts. Both devices have a TaN gate structure on a 15-nm-thick HfO_2 gate insulator layer.

Fig. 1 shows the conventional (type IV) and proposed (type V) MOS-HEMT devices. For all devices, gate length (L_G), gate–source distance (L_{GS}), gate–drain distance (L_{GD}), and width were 3, 3, 10, and 50 μm, respectively. Electron mobility and sheet carrier concentration of the two-dimensional electron gas (2DEG) channel, measured by the Hall method, were 1740 cm^2/V s and 6.81×10^{12} cm^{-2}, respectively.

Mesa isolation using BCl_3- and Cl_2-based inductively coupled plasma-reactive ion etching was performed to define active regions for all devices. After 20/80-nm-thick Ti/Al were deposited on source and drain regions by an e-beam evaporation, 100-nm-thick TaN was sputtered on the Ti/Al stack sequentially with utilizing the identical photo-resist pattern and then the whole Ti/Al/TaN stack was lifted off. The sputtering of TaN was carried out at room temperature and a working pressure of 1 m Torr under an Ar flow of 20 sccm. The sputtering power of TaN was 50 or 350 W. Then, the Ti/Al/TaN stack in the proposed device (type V) was annealed at three different temperatures of 780, 880, and 980 °C for 40 s, respectively, by rapid thermal annealing. As a gate insulator, 15-nm-thick HfO_2 was sputtered on the conventional (types III and IV) and proposed (type V) MOS-HEMTs. The specific process conditions and characteristics of sputtering HfO_2 were reported [3]. We optimized the sputtering conditions of HfO_2 so that the interface trap density (D_{it}) of 6×10^{12} cm^{-2} eV^{-1} was obtained at 0.3 eV below the AlGaN conduction band. The D_{it} is higher than the state of the art [15,16] but that is rather less than the other result [17]. In addition, a merit of the sputtering such as a fast deposition rate for thick-film applications would be also considered.

Finally, a 43-nm-thick TaN gate was sputtered on the HfO_2 gate insulator at 1 m Torr as a gate electrode. The sputtering power of the TaN gate was 50 or 350 W. The working pressure of 1 m Torr during TaN sputtering was chosen because of the lowest sheet resistance, 24.3 Ω/□ of TaN. The sheet resistance of the TaN layer increased when working pressure increased. We fixed the pressure at 1 m Torr, which was the minimum pressure for our sputtering system. Identical mesa etching was completed for the conventional devices (types I, II, III, and IV). The thickness of Ni/Au at the gate was 30/150 nm, using the e-beam evaporator. The thickness of Ti/Al/Ni/Au at the source and drain was 20/80/20/100 nm, employing the e-beam evaporator.

3. Experimental results

Electrical characteristics for the four devices (types I, II, III, and IV) were measured to investigate the sputtering power and post-annealing of TaN. Fig. 2(a) shows the measured drain leakage current of the conventional HEMTs using a Ti/Al/Ni/Au ohmic contact. The Ni/Au gate (type I) and TaN gate (type II) formed on the GaN surface. Neither device includes a gate insulator layer. A gate–source voltage (V_{GS}) of −10 V was applied to deplete the 2DEG channel under the gate. The drain leakage current was measured while increasing the drain–source voltage (V_{DS}) from 0 to 100 V. The TaN-gate HEMT (type II) exhibited a drain leakage current of 2.3 mA/mm at a V_{DS} of 100 V, which is higher than the 192 μA/mm for the Ni/Au-gate HEMT (type I) at a V_{DS} of 100 V. Additionally, the TaN/GaN Schottky barrier height was relatively low due to the low work function of TaN compared to Ni [14]. This means that a high-quality gate insulator is required to suppress the leakage current under the gate electrode.

Fig. 2(b) shows the measured drain leakage current of the conventional MOS-HEMTs with Ti/Al/Ni/Au ohmic contacts. The MOS-HEMTs with 15-nm-thick HfO_2 exhibit a low leakage current. At a V_{DS} of 100 V, the TaN-gate MOS-HEMT (type IV) with 50 W shows a drain leakage current of 17.4 pA/mm, which is less than the 67 pA/mm leakage current of the Ni/Au-gate MOS-HEMT (type