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Analysis of off-state leakage mechanisms in GaN-based MIS-HEMTs: Experimental data and numerical simulation

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ABSTRACT

This paper presents an extensive analysis of the off-state conduction mechanisms in AlGaN/GaN Meta–Insulator–Semiconductor (MIS) transistors. Based on combined bi-dimensional numerical simulation and experimental measurements, we demonstrate the following relevant results: (i) under off-state bias conditions, the drain current can show a significant increase when the drain bias is swept up to 600 V; (ii) several mechanisms can be responsible for off-state current conduction, including band-to-band tunneling and impact ionization; (iii) two-dimensional numerical simulations indicate that band-to-band tunneling plays a major role, while impact ionization does not significantly contribute to the overall leakage. Temperature-dependent *I–V* measurements were also carried out to identify the origin of the vertical drain-bulk leakage.

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1. Introduction

GaN power transistors have recently demonstrated to be excellent candidates for application in the next-generation power conversion systems. Given the high breakdown field (3.3 MV/cm), the large energy gap (3.4 eV), and the high saturation velocity (2.5×10^7 cm/s) of *GaN*, *GaN*-based High Electron Mobility Transistors (HEMTs) can operate in a large temperature range (up to 500 °C), and at high voltage levels (breakdown voltages >1 kV). Moreover, thanks to the low *on-resistance* × *gate-charge* product, these devices can reach very high operating frequencies, while having low switching losses.

Recently, several authors have demonstrated that when *GaN*-HEMTs are biased in off-state conditions with high drain voltages (up to 600 V), the sub-threshold drain current may considerably increase and reach relatively high values in the order of 100 μA/mm to 1 mA/mm; these are usually considered as the maximum current levels that can be reached by a transistor in off-state [1]. Such sub-threshold current components may originate from punch-through [2,3], reverse-leakage of the gate-drain junction [4], surface leakage [5], and vertical (drain-bulk) leakage [6,7]. In addition, several physical mechanisms can contribute to off-state current conduction, including band-to-band tunneling [8] and impact ionization [9]. High sub-threshold current components therefore limit the maximum voltage that can be applied to a transistor; for this reason, it is very important to understand how the individual conduction mechanisms listed above contribute to the overall drain leakage current, and develop models to simulate the electrical characteristics of the devices in off-state. Another important problem originates from the fact that, even in MIS-HEMTs, the sub-threshold characteristics of HEMTs devices can significantly change in response to temperature variations. Temperature-dependent characterization represents a powerful tool for study the limits of *GaN*-based transistors, and to understand how the electrical behavior of these devices changes in the typical operating temperature range (from room temperature up to 150 °C).

The aim of this paper is to contribute to the understanding of the sub-threshold current conduction mechanisms in *GaN*-based transistors. Based on combined two-dimensional numerical simulations and temperature-dependent characterization of MIS-HEMT devices, we analyze the origin of sub-threshold current; more specifically, we show that when the devices are biased in off-state, sub-threshold leakage is mostly due to band-to-band tunneling, while impact ionization effects are very limited. In

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addition, we demonstrate that for moderate drain voltages the sub-threshold current flow is confined in the *GaN* channel layer; on the other hand, for drain voltages higher than 200 V, electrons start to be transferred into the *AlGaN* back barrier layers, thus creating a further parasitic leakage path. The last part of the paper describes the temperature-dependence of the *I–V* curves of the devices, by separately investigating the individual contribution of gate, source and bulk current to the overall leakage.

2. Experimental details

The study was carried out on GaN-based metal–insulator–semiconductor transistors (MISHEMTs), with the structure schematically shown in Fig. 1. The devices are based on an AlGaN/GaN/AlGaN heterostructure grown on a 150 mm *Si* substrate by metal–organic chemical vapor deposition on top of a 200 nm AlN nucleation layer. The device structure consists of 450 nm of $Al_{0.7}Ga_{0.3}N$ followed by 800 nm of $Al_{0.4}Ga_{0.6}N$, and 1050 nm of $Al_{0.18}Ga_{0.82}N$. The growth was then continued with 150 nm of an unintentionally doped GaN channel and a 10 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. The gate insulator was composed by a 10 nm in situ grown Si_3N_4 layer and a 5 nm Al_2O_3 layer. Device passivation was obtained through a 120 nm low-pressure chemical vapor deposited (LPCVD) nitride layer. Ohmic contacts were formed by etching the triple dielectric stack $Si_3N_4/Al_2O_3/Si_3N_4$. The gate was formed by selective removal of the LPCVD nitride using Al_2O_3 as an etch stop layer, followed by the deposition and dry etching of the 30/20/250 nm W/Ti/Al gate metal stack. A gate-connected field plate was formed by extending the gate metallization by 1 μm to the drain side and 0.5 μm on the source side. The process was completed by Al and Cu interconnect metallization layers. The device geometry consists of multiple fingers with a 200 μm of total gate width. The source-gate and gate-drain separations are 1.25 μm and 9.5 μm, respectively, while the gate length is 1.5 μm.

The presence of the AlGaN buffer layers enhances the confinement of the electrons in the channel. In fact, the large polarization-induced electric field in the AlGaN layer raises the conduction band edge of the bottom of the GaN channel layer with respect to the upper SiN/AlGaN interface, creating a potential barrier against carrier diffusion in the substrate layer. This property is highlighted in Fig. 2, showing the conduction band profile of the simulated device at $V_{GS} = 0$ V, $V_{DS} = 0$ V. More details on the analyzed device can be found in [10], where all the characteristics of the sample used to obtain the experimental data are reported.

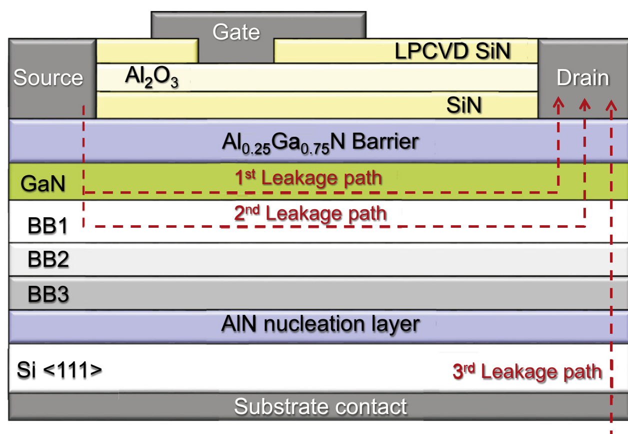

Fig. 1. Cross-section of the analyzed device.

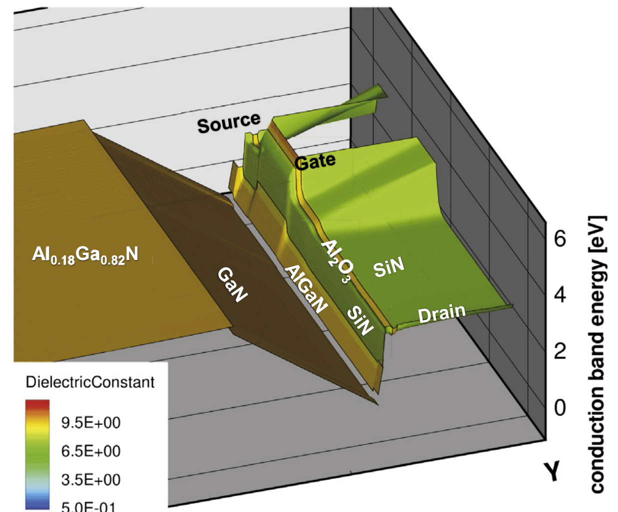

Fig. 2. Conduction band of the investigated MISHEMT.

3. Analysis of drain current components

The analysis of the sub-threshold drain current components was carried out by combined experimental measurements and numerical simulations. The simulations were carried out with the Sentaurus software [11].

One of the most critical parameters is the amount of charge that must be placed in correspondence of each heterointerface to take into account the polarization charges of AlGaN and GaN. The corresponding sheet charge densities were calculated by following the formulation described in [12]. According to [13], positive surface traps were also added, in order to have a correct modeling of device structure and fit the electrical characteristics. The validity of the model was verified by comparing the simulated I_D–V_G characteristics with the corresponding experimental data. As shown in Fig. 3, the simulation results are in good agreement with the measured curves. The threshold voltage of the analyzed devices is approximately equal to −5.5 V.

The sub-threshold (off-state) current measurements were carried out at two gate voltage levels, both smaller than the threshold voltage: $V_G = V_{TH} - 0.5$ V and $V_G = V_{TH} - 2$ V. While keeping the

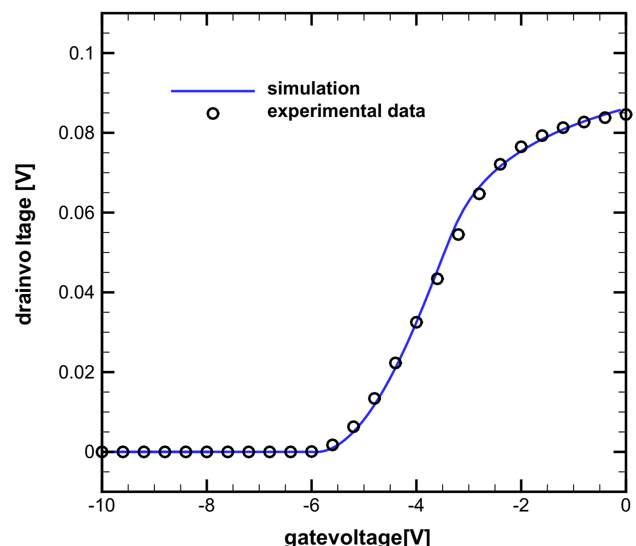

Fig. 3. Drain current - drain voltage characteristic for $V_D = 4$ V.

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