Solid-State Electronics 113 (2015) 28–34

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Physics-based stability analysis of MOS transistors ☆

A. Ferrara [a,*], P.G. Steeneken [b,c], B.K. Boksteen [a], A. Heringa [b], A.J. Scholten [b], J. Schmitz [a], R.J.E. Hueting [a]

[a] MESA+ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands
[b] NXP Semiconductors, The Netherlands
[c] Delft University of Technology, Delft, The Netherlands

ARTICLE INFO

Article history:
Available online 10 June 2015

Keywords:
Power MOSFET
Silicon-on-insulator (SOI)
Safe Operating Area (SOA)
Safe Operating Volume (SOV)
Stability factor
Failure function

ABSTRACT

In this work, a physics-based model is derived based on a linearization procedure for investigating the electrical, thermal and electro-thermal instability of power metal–oxide–semiconductor (MOS) transistors. The proposed model can be easily interfaced with a circuit or device simulator to perform a failure analysis, making it particularly useful for power transistors. Furthermore, it allows mapping the failure points on a three-dimensional (3D) space defined by the gate-width normalized drain current, drain voltage and junction temperature. This leads to the definition of the Safe Operating Volume (SOV), a powerful frame work for making failure predictions and determining the main root of instability (electrical, thermal or electro-thermal) in different bias and operating conditions. A comparison between the modeled and the measured SOV of silicon-on-insulator (SOI) LDMOS transistors is reported to support the validity of the proposed stability analysis.

1. Introduction

In power transistors, failure is often associated with instability, which causes one or more device parameters, such as current, voltage or temperature, to runaway [1]. Stability can be experimentally investigated by measuring the device characteristics close to the failure limit [2–6]. This allows calculation of a stability factor that is a measure of the device sensitivity to runaway. However, such a procedure has two drawbacks: (1) it can affect the device performance by changing parameters such as threshold voltage, on-resistance and breakdown voltage and (2) it detects the occurrence of instability but not its physical origin (electrical or thermal).

In order to overcome the first drawback, physics-based models [2,3,5,7,8] or TCAD simulations [9] have been used to predict and quantify instability. However, modeling and simulating runaway effects causes the output parameters to diverge and makes it difficult to identify the physical origin of the numerical instability.

The physics-based stability analysis can be used to identify the boundary between electrical and thermal failure mechanisms in LDMOS transistors (Fig. 1), hence to distinguish the root cause of device failure [10]. In comparison to our earlier work [10], the derivation of the stability factors is elaborated with further mathematical detail, making it generally applicable to any kind of MOS transistor. The electrical and thermal stability factors are defined assuming that self-heating does not play a role in the electrical runaway, while avalanche breakdown and the internal parasitic bipolar transistor of the MOS transistor do not affect thermal stability.

Device failure can be related to an electro-thermal stability factor that includes both the electrical and thermal failure mechanisms (Fig. 2). The individual analysis of runaway mechanisms allows determination of the relative contributions of electrical and thermal phenomena to failure, thus identifying the primary cause of runaway. This knowledge allows one to determine, depending on the operating conditions, whether the electrical or thermal device properties, or both, need to be improved to increase the so-called Safe Operating Area (SOA), *i.e.* the two-dimensional (2D) frame work in the current–voltage plane where it is safe to operate the LDMOS [11,12].

The stability equations need to be combined with models of the different MOS current contributions (intrinsic MOS current I_{dMOS}, bipolar base and collector currents I_b and I_c, and impact ionization current I_{ii}) including their temperature dependencies. For this purpose analytical models for MOS transistors, TCAD simulations, experimental data or combinations can be used [2,3,5,7–9,13]. In this work, physics-based analytical expressions [14,15] with experimental [6] fitting parameters have been used (Appendix A). As shown in [10] for SOI LDMOS transistors, the proposed model

☆ This work is a part of the Dutch Point-One program and is supported financially by Agentschap NL, an agency of the Dutch Ministry of Economic Affairs.
* Corresponding author.
E-mail address: a.ferrara@utwente.nl (A. Ferrara).

http://dx.doi.org/10.1016/j.sse.2015.05.010
0038-1101/

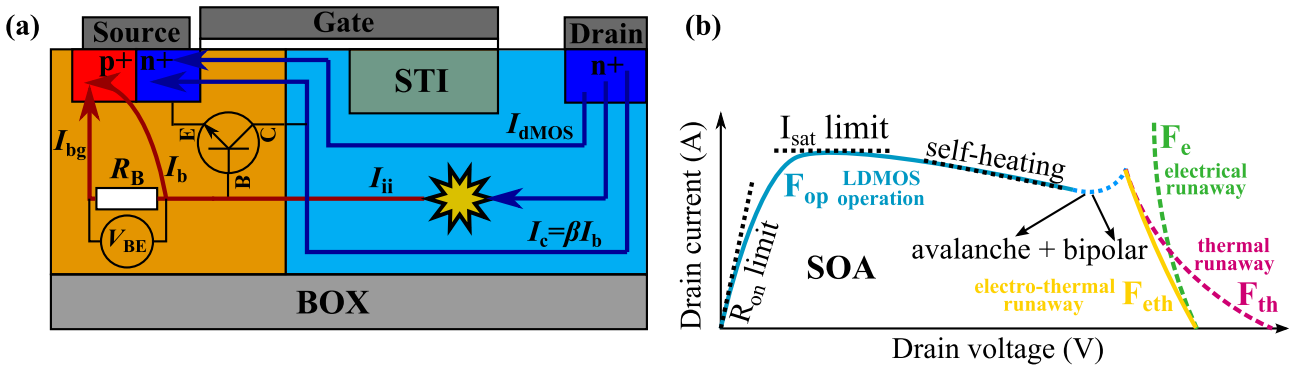

Fig. 1. (a) Parasitic bipolar and avalanche multiplication in the operation of an LDMOS transistor. (b) Schematic of the Safe Operating Area (SOA), showing the failure and operating functions which are analytically investigated in this work.

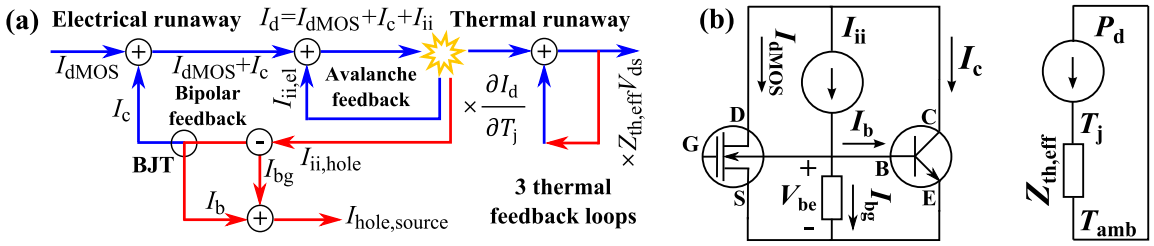

Fig. 2. (a) Schematic representation of the origin of electrical and thermal runaway. (b) Electro-thermal circuit model of the MOS-bipolar system.

allows mapping the failure points onto a 3D space defined by the gate-width normalized drain current, drain voltage and junction temperature. This leads to the definition of the failure functions and the introduction of the Safe Operating Volume (SOV).

2. Origin of electro-thermal runaway

A general overview of the positive electrical and thermal feedback mechanisms leading to instability and runaway is provided in Fig. 2. At high drain voltages V_{ds}, the MOS electron current I_{dMOS} generates electron–hole pairs contributing to an impact ionization current I_{ii} with an electron and a hole component. The electrons flow towards the highly doped n^+ drain contact, the holes flow towards the p^+ body contact inducing a voltage drop V_{be} over the base resistance R_B. This switches on the internal parasitic bipolar with a base current I_b and a corresponding collector current $I_c \approx \beta I_b$, where β is the current gain. This current I_c is in turn multiplied by avalanche when flowing in the drift extension, resulting in a positive feedback behavior. Self-heating [5,8,16] is included in the model by introducing an effective thermal impedance $Z_{th,eff} \approx (T_j - T_{amb})/P_d$ [6], where it is assumed for simplicity that the dissipated power P_d is independent of the pulse time t_{pulse}.

Electrical failure occurs because of the interaction of the parasitic bipolar with the current I_{ii}. Part of this current flows through the base of the bipolar and contributes to $I_c \approx \beta I_b$, which is avalanche multiplied and fed back into the base. Thermal failure can occur because of thermal runaway in each of the current components I_{dMOS}, I_c or I_{ii}. The temperature coefficient of I_{dMOS} depends on V_{gs} [17], I_{ii} has a slightly-negative temperature coefficient [18] (not included in the model), and I_c has a positive temperature coefficient [19]. In most cases, the increase in I_c (also including thermal leakage) induced by self-heating determines thermal instability [2,3,5,8]. However, for V_{gs} below the zero-temperature coefficient point, I_{dMOS} also contributes to instability [5,8,17].

For studying the failure mechanisms the so-called stability factors [1] are required. The complete derivation of the stability factors is carried out in Section 3. Although electrical and thermal failure mechanisms often both play a role in transistor failure, their relative contributions can be identified using the analytical stability analysis described in the same section. The electro-thermal behavior of the MOS transistor is described by combining the electrical and thermal contributions to stability in a coupled equation system. The large signal behavior of the MOS transistor including the parasitic bipolar transistor and self-heating can be described as follows:

$$\begin{cases} I_{dn} = M \cdot \frac{(I_{dMOS}+I_c)}{W_{gate}} = f_e(V_{gs}, V_{ds}, V_{be}, T_j) & \text{(a)} \\ T_j = T_{amb} + Z_{th,eff}(t_{pulse}, A) W_{gate} V_{ds} I_{dn} & \text{(b)}, \end{cases} \quad (1)$$

where I_{dn} is the drain current per unit gate width W_{gate}, I_{dMOS} is the internal MOS drain current, V_{gs} the gate-source voltage, V_{ds} is the drain-source voltage, V_{be} is the base-emitter voltage, T_j is the junction temperature, and T_{amb} is the ambient temperature. The effective thermal impedance $Z_{th,eff}$ depends on the pulse time t_{pulse} and the device area A, and the multiplication factor M is a parameter that is a measure for the increased drain current caused by impact-ionization. The function f_e describes the electrical operation of the MOS-bipolar system depending on the applied biasing and junction temperature T_j. It can be constructed based on compact modeling, TCAD simulations or measurements on special test structures including a temperature sensor and/or a separate body contact. Hence, the electro-thermal behavior of the MOS transistor is described by (1) in case of large signal biasing.

3. Analytical stability analysis

3.1. Derivation of the electrical stability factor

In order to quantify the relative contributions of electrical [20] and thermal [5,8] runaway to coupled electro-thermal [2,9,21] failure mechanisms, analytical stability equations are derived following a linearization procedure. In this section, it is shown how the