Solid-State Electronics 113 (2015) 116–120

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Flexible and stretchable electronics for wearable health devices

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ARTICLE INFO

Article history:
Available online 14 June 2015

Keywords:
Flexible electronics
Stretchable electronics

ABSTRACT

Measuring the quality of human health and well-being is one of the key growth areas in our society. Preferably, these measurements are done as unobtrusive as possible. These sensoric devices are then to be integrated directly on the human body as a patch or integrated into garments. This requires the devices to be very thin, flexible and sometimes even stretchable. An overview of recent technology developments in this domain and concrete application examples will be discussed.

1. Introduction

Today's weaable healthcare tools are complex systems, based on advanced electronics (mixed-signal front-ends, DSP, transceiver, power management, memory). Nevertheless, they predominantly rely on rather traditional system design and technology for integration and packaging. These devices are typically built using conventional board-level and/or package-level integration. The result is mostly a system that is uncomfortable to wear because it is rigid, large and heavy. From a user point of view, the device should preferably be comfortable and unnoticeable. Standard integration technologies typically not fulfill these requirements.

An interesting approach to achieve better wearability is by transforming the flat rigid device into a flexible or stretchable electronics device that can better follow the shape of the human body.

The current paper addresses recent technology developments at our institutes that enable this. Two generic complementary platforms will be discussed. The first one is based on organic and large area electronics (OLAE) technologies. It is specifically targeting low cost, large area devices like health patches. The second one is based on thin film technologies. This platform targets more advanced wearable and medical devices. The paper also addresses progress in two complementary technologies that are used in both platforms: thin chip integration and a technology for realizing stretchable devices from flexible foils. Finally, concrete application prototypes will be shown in which the platforms and technologies are being exploited.

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http://dx.doi.org/10.1016/j.sse.2015.05.024
0038-1101/

2. Technology advancements

2.1. Organic and large area electronics platform

Organic and large area electronics (OLAE) are built on thin and flexible plastic foils. Mostly polyesters like PET and PEN are chosen because of their low cost and transparent nature. A large part of the electronic functionality is printed as thin layers using functional inks. The end result is a very thin and flexible but also cost effective electronics device. OLAE technologies are currently already being industrially employed for wearable health and medical devices – for example for ECG patches but also for glucose diagnostic devices. Up to now this primarily concerns devices having a low complexity. Only coarse pitch circuitry traces are being printed while all more complex functionality (e.g. microcontrollers, radio chips) is integrated into the system on a separate, often rigid, printed circuit board (PCB).

Recent advances in materials, technologies and processes enable the realization of more complex devices using OLAE technologies.

Screen printing and inkjet printing [1] are the most commonly used printing techniques in OLAE. Of these two, screen printing is the most appropriate for the wearable health and medical devices as considered in this paper. As compared to inkjet printing it more easily enables the realization of complex multilayer circuits and the printed structures typically have a better conductivity owing to a thicker print deposit.

Circuitry patterns with resolutions down to 50 μm line/spacing can routinely be achieved. These resolutions are well in-line with what is needed for wearable health and medical devices. An example of such a fine line printed pattern is given in Fig. 1. It shows the fanout circuitry for a bare die silicon chip. The circuitry was printed

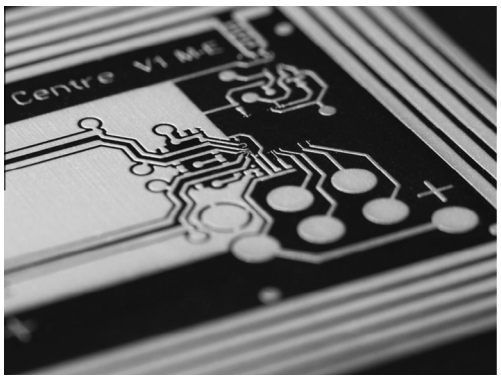

Fig. 1. Example of a printed circuitry pattern. Shown is a fanout circuitry for a bare die silicon chip. At the bonding position of the chip, the circuitry was printed at a minimum pitch of 100 μm (50 μm line and spacing).

with a nanoparticle Ag-based screen printing paste (DuPont) and using special high-resolution printing screens (SPG Prints). At the bonding position of the chip, the circuitry was printed at a minimum pitch of 100 μm (50 μm line and spacing).

Realizing more complex circuits also implies the need for multilayered circuitry patterns. Also here advances have been made in recent years. Fig. 2 shows an example of a three layer printed circuit by printing alternating layers of conducting (gray) and dielectric ink (white) on top of each other.

Fig. 2 also emphasizes one of the clear advantages of OLAE technologies: the base foil has a thickness of only 50 μm while the 5 sequentially printed layers (conductors, dielectrics) only add a maximum of 35 μm to the thickness. This results in a very flexible 3 circuit layer PCB having a thickness of less than 150 μm.

2.2. Thin film electronics platform

More complex, high-end wearable and medical devices often need device (e.g. thinness, flexibility) and circuit (e.g. pitch, IO count, conductivities) performance that cannot be achieved with OLAE technologies. Therefore, a technology platform is being developed which allows realizing complex systems or subsystems. So, not only standalone patches can be realized, but also subparts of patches, which then can be combined with OLAE, taking advantage of the complementary nature of both approaches.

The thin film electronics (TFE) platform is enabled by combining spin-on polyimide films with thin-film metallization. Polyimide films have been used as dielectric and passivation layers

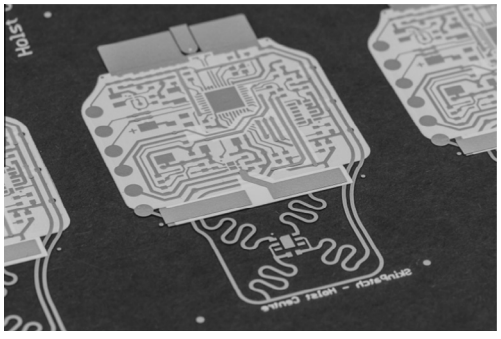

Fig. 2. Overview image of a 3 layer printed circuitry patterns on a 50 μm PET foil. Circuitry is printed with screen printing technology using Ag-filled conductive ink (gray) and dielectric ink (white).

in the microelectronics industry for many years, as they exhibit exceptional electrical, thermal and mechanical properties. Thin-film metallization offers the obvious advantage that fine-pitch metallization schemes can be realized, ensuring compatibility with interconnection pitches of conventional, commercially available dies. Vacuum deposition processes, such as sputtering or evaporation, are thus preferred techniques to metallize the polyimide films. In addition, the deposition processes allow for use of a variety of metals: copper is generally used because of its electrical conductivity, but also biocompatible alternatives such as gold or even platinum can be considered.

The process starts from a glass carrier substrate onto which a polyimide layer is spin coated and cured, resulting in a stress-free polyimide film with a typical thickness in the range of 5–10 μm. Next, thin-film copper metallization (1 μm thickness) is sputter deposited, preceded by an adhesion enhancement layer composed of titanium tungsten, deposited in the same vacuum cycle. The metallization is then patterned via a sequence of photolithography and wet etching to realize the interconnects, and covered by depositing another polyimide film. Electrical contacts are provided by selectively removing the covering polyimide film on top of specific metal pads. This is done by laser ablation, using a nanosecond KrF excimer laser (248 nm). By repeating this procedure, i.e. the sequence of metal deposition, polyimide coating and via ablation, multilayer circuitry can be enabled.

To release the devices from its carrier, a laser release methodology is used to ablate a sub-micron layer of polyimide at the glass/polyimide interface. This ablation procedure can be adapted according to the final device geometry.

2.3. Thin chip integration

Most medical and wearable devices need some form of intelligence. For example microcontrollers (to process sensor data) or radio chips (to communicate this data with the outside world). Integrated circuits are normally supplied in packaged format. Using these bulky and rigid packages has a big impact on the thickness and flexibility advantages of the base foils.

At thicknesses below 25 μm, it is known that silicon becomes flexible [2]. It would thus be preferred to integrate the needed silicon functionality as bare die and in a thinned down form. Several approaches exist to achieve thin silicon chips. Grinding and polishing is one of the more common routes but for example the ChipFilm technology of IMS Chips [2] results in inherently thin silicon chips.

The integration of these unpackaged, thinned dies is done using either of two distinct approaches.

The first approach, used in combination with the TFE platform, the ultra-thin chips are embedded with the active side facing upwards (face-up) in between two sequentially deposited spin-on polyimide layers. Although height irregularities in the order of the thickness of the die are introduced, electrical connectivity can be provided using the described processing sequence. Fig. 3 shows a typical example of this approach, in which an interconnection test die is provided with fan-out metallization. In the second approach, the active components are assembled face-down on the plastic foil. Both conductive adhesives and solders can be used to establish the interconnects.

In particular the integration of silicon chips with OLAE foils is a challenge because of the low thermal stability of the polyesters. PEN has a glass transition temperature (Tg) of ~130 °C and PET of ~85 °C while poly(imide) has a Tg of ~350 °C [3].

This limitation in thermal stability excludes many well- established processes for making electronic products, as for example soldering. The integration of silicon chips with OLAE foils is most commonly done using a flip chip process based on conductive