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Superior performance and Hot Carrier reliability of strained FDSOI nMOSFETs for advanced CMOS technology nodes

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The Hot Carrier (HC) reliability of NMOS transistors fabricated on biaxially tensile-strain SOI substrates (sSOI) is compared to that of devices fabricated on standard unstrained SOI substrates. It is shown that sSOI-based devices not only exhibit a 10% higher performance in term of I_{ON}/I_{OFF} but also show superior HC reliability at same drive current. This reliability improvement may be explained by a better interface quality for sSOI films.

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1. Introduction

With the approaching end of conventional planar bulk CMOS scaling and the need to continue the roadmap below 20 nm, semiconductor industry is moving to new transistor architectures like FinFETs or FDSOI. Among these emerging technologies, FDSOI is a major option because it combines the simplicity of the planar integration scheme used for Bulk technology with the electrostatic efficiency of FinFET technology. Furthermore, SOI enables an efficient strain engineering of the channel and Source/Drain engineering to boost transistor performance. Particularly, strain SOI (sSOI) is a promising candidate for sub-10 nm nodes since it was demonstrated to significantly improve the drive current of nMOSFETs [1,2]. Nevertheless, this performance booster may affect the Hot Carrier (HC) reliability of the device. Indeed it was shown recently that, in deeply scaled technologies, the degradation due to Hot Carriers generated close to the drain is directly proportional to the drive current flowing through the transistor [3]. Therefore an improvement of the drain current combined to an increase of the lateral electric field in short channel devices might degrade the HC reliability of the strained SOI MOSFET compared to their unstrained SOI counterparts [4–6].

In this paper, we investigate the impact of strained Si layer on the performance and the HC reliability of FDSOI transistors. First, we compare the performance of FDSOI devices fabricated on sSOI and SOI substrates. Then HC degradation is thoroughly investigated for both architectures. Drifts of all common MOSFET parameters affected by HC effects are carefully analyzed to identify the defects responsible for HC degradation in both cases *i.e.* interface states and/or oxide trapping. The change in the material bandgap and properties, induced by the strain technology is used to explain sSOI reliability improvement. Finally, HC lifetime of these two kinds of transistors is evaluated.

2. Technology and devices

NMOSFETs were fabricated using a Gate First integration scheme on 300 mm SOI and sSOI substrates. In both cases, the silicon film is 7 nm thick and the buried oxide (BOX) is 145 nm thick. The dielectric stack consists of a thin HfSiON layer capped with a TiN metal gate. The Electrical Oxide Thickness (EOT) of the HK/MG stack is 1.2 nm. The channel length (L_G) varies from 100 nm down to 30 nm length. The transistor width (W) is fixed to 10 μm.

Both SOI and sSOI substrates were fabricated with Smart Cut™ technology. In the case of sSOI, the strain Si film (sSi) is grown on a relaxed $Si_{0.8}Ge_{0.2}$ buffer layer before being transferred on a handle substrate. The resulting tensile strain in the sSi film is evaluated to

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+1.36 GPa. After bonding and transfer, the residual SiGe buffer layer is removed by selective etch. sSOI is a single layered, completely Ge-free "on insulator" substrate (Fig. 1).

3. Tests conditions

To evaluate the benefit of sSOI films, electron mobility was extracted on large and long channel transistors (L_G = 10 µm, W = 10 µm) using the split CV technique. The standard $I_D(V_G)$ measurements were performed on transistors with different gate length to evaluate the threshold voltage V_{th} at constant drain current $I_D = 10^{-7} * (W/L_G)$ and the I_{ON}/I_{OFF} ratio at V_{DD} = 1 V. For Hot Carrier degradation, we used standard JEDEC specifications. Stress and measurement tests were performed at 125 °C unless otherwise specified. NMOSFETs with different L_G are stressed at different voltages V_{stress} from 1.4 to 2 V during 1000 s, in worst case conditions $V_{stress} = V_G = V_D$ (Figs. 2 and 3) [7]. Between each stress sequence, we recorded the drifts of the key MOSFET parameters *i.e.* the threshold voltage V_{th}, the transconductance peak $g_m{}^{max}$ in the linear regime ($V_{D,meas}$ = 50 mV) and the saturated drain current $I_D{}^{sat}$ at $V_{D,meas} = V_{DD}$ = 1 V. The corresponding criteria associated to each parameter for a 10 years device lifetime are 50 mV of V_{th} shift, 10% of $g_m{}^{max}$ degradation and 10% decrease of $I_D{}^{sat}$ drift respectively.

Finally, dedicated fast current measurements, where the whole $I_D(V_G)$ characteristic is measured in ~5 µs, were performed to monitor the degradation and relaxation of the same parameters in order to avoid any recovery effects.

4. Measurement results and discussion

4.1. Performance of SOI and sSOI transistors

Fig. 4 shows a comparison of electron mobility in SOI and sSOI nMOSFETs extracted by split CV technique. As expected, strain strongly improves mobility μ_n in long channel devices in the whole range of vertical effective field. The maximum gain obtained around the mobility peak is remarkable, reaching 77%. The benefit of strain is reduced for short-channel devices as depicted in Fig. 5. This may result from several combined effects as (1) a difference in

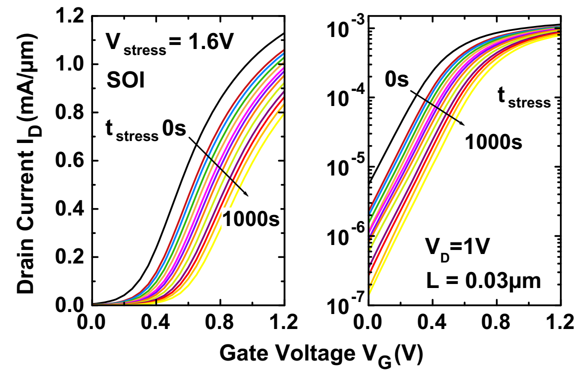

Fig. 2. Degradation of the $I_D(V_G)$ characteristic with stress time t_{stress} for the shortest gate length transistor at high stress voltage (linear and logarithmic scale). This measure is used to extract the $I_D{}^{sat}$ degradation required for the HC lifetime extrapolation.

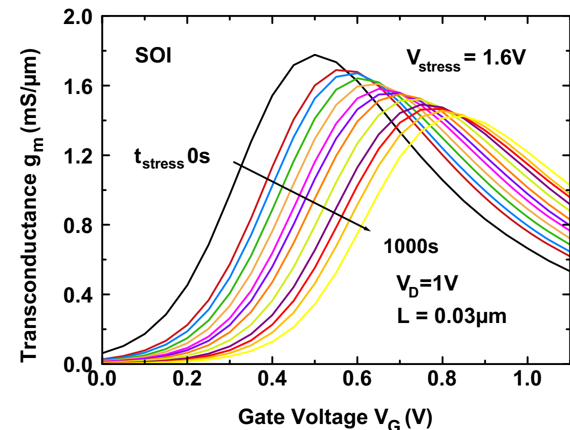

Fig. 3. Degradation of the transconductance curve with stress time t_{stress} for the shortest gate length NMOS transistor at $V_{D,stress} = V_{G,stress}$ = +1.6 V. These curves are used to extract the g_m^{max} degradation required for the HC lifetime extrapolation.

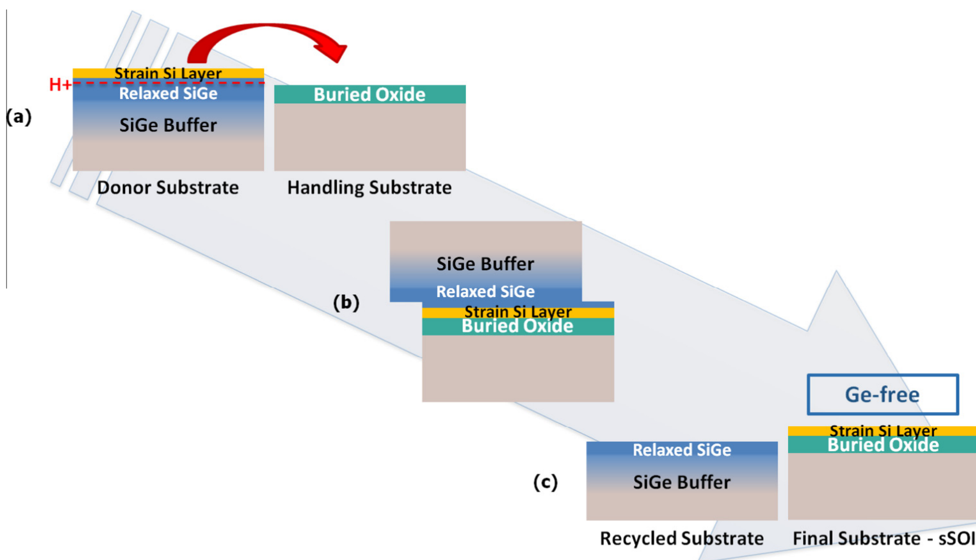

Fig. 1. sSOI substrate fabricated by Smart Cut™. (a) Strain silicon (sSi) film grown on relaxed $Si_{0.8}Ge_{0.2}$ buffer leading to +1.36 GPa tensile strain. Hydrogen is implanted into SiGe buffer (dotted line) and buried oxide (BOX) is grown on handling substrate. (b) Donor substrate is bonded to handling substrate and separation at implantation depth, leaving the strained silicon layer and (c) etching of residual SiGe layer on final substrate and recycling of donor wafer.

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