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Impact of the array background pattern on cycling-induced threshold-voltage instabilities in nanoscale NAND Flash memories

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ABSTRACT

This paper highlights that cycling-induced threshold-voltage instabilities in nanoscale NAND Flash technologies display a non-negligible dependence on the background pattern of the memory array during idle/bake periods. Experimental results clearly reveal, in fact, that instabilities in a (victim) cell do not depend only on its memory state, but also on the memory state of its first neighboring (aggressor) cells. The magnitude of this new cell-to-cell interference effect, moreover, appears to depend on the memory state of the victim cell, decreasing with the increase of its threshold-voltage level. From all of the gathered experimental evidence a physical picture explaining the phenomenon is provided, which is, finally, confirmed with the help of numerical simulations.

1. Introduction

Cycling-induced threshold-voltage (V_T) instabilities represent one of the most relevant reliability issues for nanoscale NAND Flash memories. Instabilities are mainly the result of charge detrapping from the tunnel oxide of the memory cells, giving rise to unwanted displacements of their V_T during idle/bake periods [1–8]. Although the statistical nature of the detrapping process and, in turn, of the resulting V_T shift (ΔV_T) has been clearly recognized [3,6,9,10], an average reduction of V_T as time elapses is the typical feature of detrapping in Flash arrays, owing to a dominant neutralization of negative charge in the cell tunnel-oxide [3–5,7]. This negative ΔV_T is particularly detrimental for multi-level devices where the increase of storage density is traded off with the reduction of noise margins [11].

In this paper, extending what presented in [12], we provide experimental evidence showing that the average ΔV_T ($\langle \Delta V_T \rangle$) coming from detrapping in a nanoscale NAND Flash array does not depend only on the memory state of the cells being monitored (*victim cells*), but also on the state of their first neighboring cells (*aggressor cells*). In particular, experimental results show that the $\langle \Delta V_T \rangle$ of the victim cells increases when their aggressor cells are on a higher V_T level. This represents an additional interference effect among the cells of a state-of-the-art NAND Flash array, whose magnitude appears rather strong when victim cells are on a low V_T state. From the collected experimental results, a physical picture explaining the phenomenon is provided and validated with the help of 3-Dimensional (3-D) numerical simulations.

2. Experimental results

2.1. Test scheme

We investigated the $\langle \Delta V_T \rangle$ coming from charge detrapping during post-cycling bake experiments on our 20 nm multi-level NAND Flash technology [11]. To this aim, a total number of 10 k program/erase cycles were first performed on a memory block, randomly moving the cells from the erased (E) state to one of the three possible programmed levels of the device (namely, from lowest to highest, $L1$, $L2$ and $L3$). At the end of cycling, a random background pattern (BP) was created in the array and V_T instabilities were monitored during a bake test at $T_B = 125$ °C. In order to explore the BP sensitivity of $\langle \Delta V_T \rangle$, the entire array V_T map was periodically gathered by stopping the bake experiment, cooling the sample down to room temperature and accomplishing read operations on all of the array cells. From the array V_T maps, the ΔV_T of each cell was then extracted as a function of the bake time t_B and the $\langle \Delta V_T \rangle$ of cells in the same initial (pre-bake) state and with the same BP of aggressor cells was calculated. The definition of victim and aggressor cells in the NAND array is highlighted in Fig. 1: each cell in the array was considered a victim cell

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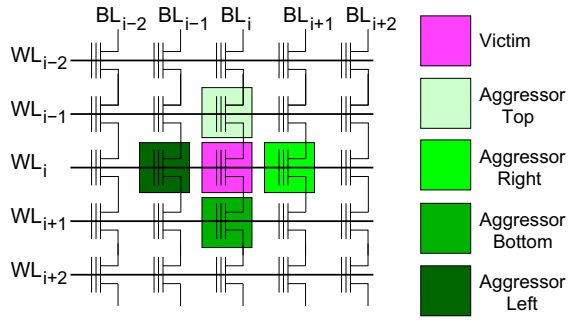

Fig. 1. Schematics for cell connection in the NAND array, highlighting a victim cell and its four neighboring aggressor cells. The BP given by the aggressor cells will be indicated in the following keeping the order: top, right, bottom, left.

surrounded by four aggressor cells placed at its top, right, bottom and left (the BP resulting from the state of the aggressor cells will be indicated keeping this order from now on).

2.2. Uniform background patterns

Fig. 2 shows the $\langle \Delta V_T \rangle$ transient of the victim cells on level $L1$ (a), $L2$ (b) and $L3$ (c) having a uniform BP of aggressor cells around them during the bake experiment. A relevant BP sensitivity of V_T instabilities during bake clearly appears for victim cells on $L1$, with an increase of $\langle \Delta V_T \rangle$ moving from the E,E,E,E to the $L3,L3,L3,L3$ BP. The pattern sensitivity, however, decreases for victim cells on level $L2$ and almost vanishes for victim cells on level $L3$.

In order to investigate more in detail the BP sensitivity of Fig. 2, we fit the $\langle \Delta V_T \rangle$ transients according to the following logarithmic trend [5]:

$$\langle \Delta V_T \rangle = -\alpha \cdot \ln\left(1 + \frac{t_B}{t_B^*}\right) \quad (1)$$

where t_B^* is the equivalent time elapsed between the end of cycling and the first read operation on the array [5]. From the fitting, the slope α of the logarithmic trend can be extracted as a function of the state of the victim and of the aggressor cells, as shown in Fig. 3. Results reveal, first of all, the typical increase of α with the initial V_T level of the victim cells [5], coming from a dependence of the detrapping rate on the electric field in the cell tunnel-oxide during bake. Besides, results clearly highlight that the value of α of the victim cells on level $L1$ increases by about a factor of 2.5 when moving from the E,E,E,E to the $L3,L3,L3,L3$ BP of the aggressor cells. This increase is, instead, only of about a factor of 1.5 and 1.2 for the victim cells on level $L2$ and $L3$, respectively.

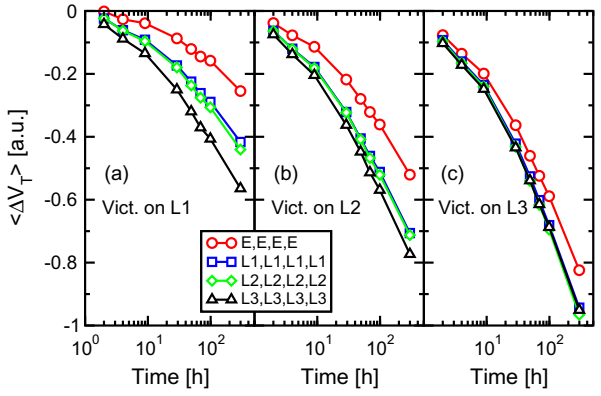

Fig. 2. $\langle \Delta V_T \rangle$ transient of the victim cells on level $L1$ (a), $L2$ (b) and $L3$ (c) when their aggressor cells are all on level E (red curve), $L1$ (blue curve), $L2$ (green curve) and $L3$ (black curve). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

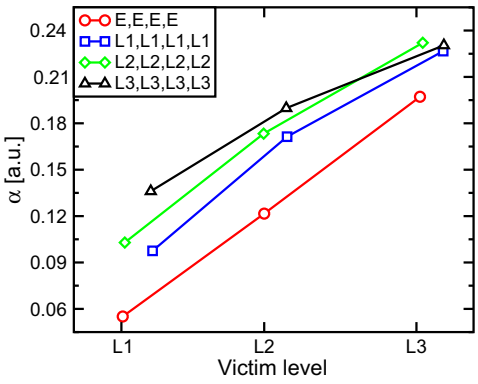

Fig. 3. Values of α resulting from the fitting of the $\langle \Delta V_T \rangle$ transient of the victim cells with (1), as a function of the state of the victim cells and for the four possible uniform patterns of the aggressor cells.

Results in Figs. 2 and 3 highlighted that the array BP has a non-negligible impact on the post-cycling data retention of the cells in a nanoscale NAND array. Note, to this regard, that the observed dependence of $\langle \Delta V_T \rangle$ on the BP is specific of the detrapping process, while different results have been reported in other working conditions for other competing mechanisms [13]. However, since the attempt to increase the number of bits per cell to improve the equivalent integration density of the memory array comes along with a reduction of its noise margins, making the differences in the $\langle \Delta V_T \rangle$ resulting from different BP in Figs. 2 and 3 largely relevant for array operation, these results confirm that a careful assessment of the reliability of nanoscale NAND Flash arrays cannot avoid, first of all, addressing different BP and, moreover, that the worst case BP may change during array lifetime. This sensitivity of cell reliability to the array BP can be considered, in general terms, a direct consequence of the closest and closest proximity of the cells in the NAND array as technology scaling proceeds, enhancing their electrostatic interaction during array operation.

2.3. Non-uniform background patterns

To gain a deeper insight on the basic phenomenology of the effect shown in Figs. 2 and 3, we investigated the $\langle \Delta V_T \rangle$ of the victim cells in the array having a non-uniform BP around them during data retention. The results obtained when only the two aggressor cells along either the bit-line or the word-line direction are on a programmed state are shown in Figs. 4 and 5, respectively. In both cases, the $\langle \Delta V_T \rangle$ transient qualitatively reveals the same BP sensitivity highlighted in Fig. 2. However, while the sensitivity remains clear and strong in the case only aggressor cells along the bit-line direction are programmed (Fig. 4), it appears largely reduced when aggressor cells along the word-line direction only are programmed (Fig. 5). This can be clearly observed also in Fig. 6, where the values of α extracted from the fitting of the transients of Figs. 4 and 5 according to (1) are reported. These results reveal that the observed cell-to-cell interference effect is mostly related to the aggressor cells in the bit-line direction. This is further confirmed by Fig. 7, showing the values of α in the case where only the aggressor cell at the bottom (a) or at the left (b) of the victim cell is programmed.

3. Physical origin of the new interference effect

3.1. Discussion

The experimental results presented in the previous section highlighted a new cell-to-cell interference effect occurring in nanoscale NAND Flash arrays and making the post-cycling V_T