Nanoelectromechanical digital logic circuits using curved cantilever switches with amorphous-carbon-coated contacts

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ABSTRACT

Nanoelectromechanical (NEM) switches have the potential to complement or replace traditional CMOS transistors in the area of ultra-low-power digital electronics. This paper reports the demonstration of prototype circuits including the first 3-stage ring oscillator built using cell-level digital logic elements based on curved NEM switches. The ring oscillator core occupies an area of 30 µm × 10 µm using 6 NEM switches. Each NEM switch device has a footprint of 5 µm × 3 µm, an air gap of 60 µm and is coated with amorphous carbon (a-C) for reliable operation. The ring oscillator operates at a frequency of 6.7 MHz, and confirms the simulated inverter propagation delay of 25 ns. The successful fabrication and measurement of this demonstrator are key milestones on the way towards an optimized, scaled technology with sub-nanosecond switching times, lower operating voltages and VLSI implementation.

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1. Introduction

CMOS has been the predominant technology for digital integrated circuits since the semiconductor industry made the transition from NMOS technology in the early 1980s. Present-day microprocessors are manufactured using a 22 nm CMOS process with a transition to 14 nm technology starting at the end of 2014 [1,2]. Continuing to shrink devices beyond the 8 nm technology node requires tremendous efforts in devices, materials and process research.

There are two fundamental issues that limit progress for ultra-low-power applications in CMOS:

1. The static leakage current of circuits built using high-performance CMOS technologies is approaching the dynamic switching current. Only a few high-performance computing applications have circuit-activity levels that contain the leakage power at a reasonable level of <10% of the active power.

The power-density limitations (∼100 W per processor for desktop applications, significantly less for embedded systems) further exacerbate this challenge.

2. The theoretical minimum for the subthreshold slope of silicon-based MOS transistors is 60 mV/decade, which leads to a minimum supply voltage of >400 mV for practical applications [3]. Among other issues, this limits the gains in power efficiency obtainable by moving to next-generation CMOS technology.

Beyond these fundamental issues, the cost of using the latest CMOS technology node has reached a point where only a few (very) high-volume applications can afford it.

Given the scaling limits of silicon-based CMOS technology, alternative devices have been proposed including, but not limited to, carbon/graphene nanostructures, molecular devices, quantum devices and photonics [1]. Of the various post-CMOS device candidates, the nanoelectromechanical (NEM) switch shows promise because it offers a simple fabrication process with fewer masks and allows co-integration with CMOS via a back-end-of-line (BEOL) process. It also addresses the aforementioned fundamental problems because the NEM switch has virtually zero leakage, and the abrupt switching characteristic (no subthreshold slope limitation) potentially allows the use of lower supply voltages [4,5].

Several research groups have been or are currently investigating the design and applications of NEM switches for logic applications, including but not limited to [6–19].

Our work involves the development of a NEM-switch-based VLSI framework that encompasses device optimization and fabrication, BEOL processing, logic design, and device-/circuit-modeling. As a first key demonstrator of our approach, we implemented a ring oscillator consisting of 3 inverting stages using in-plane curved cantilever NEM switches coated with amorphous carbon (a-C) on the contact. The in-plane design is the basis to achieve the design freedom required for curved cantilevers. It also solves many of the scalability issues that out-of-plane switches face, because the critical air gap is defined through a single vertical etching step. The switches have been developed for digital logic applications and feature a curved cantilever design for improved robustness over straight cantilevers [20,21]. Nanoscale conducting filaments are formed within the a-C contact material via Joule heating through the application of a sufficiently high voltage without creating large adhesion forces.

The reduced adhesion forces between the two a-C-coated contacts allow control of the hysteresis of the switch and, together with the inherent stability of the material, improve reliability [21]. A dedicated output stage has been developed to safely interface the NEM switch circuits with the large capacitive load of the external measurement equipment. The experimental measurements have shown the successful operation of a standalone single-stage inverter, a buffer, and a 3-stage ring oscillator operating at a frequency of 6.7 MHz. The measurements are consistent with simulations from both finite-element analysis and analytical compact modeling of the curved NEM switch.

The remainder of this paper is structured as follows: Section 2 describes the general features of our 3-terminal NEM switch and how it is fabricated. Section 3 discusses our approach to bringing our devices to the level of VLSI implementation, including the BEOL integration process, standard cell design, interface circuits, and device/circuit modeling. Section 4 details prototype circuits we have fabricated and measured. We also show how well our measurement results align with our simulations. Finally, we conclude the paper in Section 5.

2. NEM switch device

2.1. Device characteristics

As shown in Fig. 1, the NEM switch is designed using an in-plane curved cantilever approach, which provides a compact footprint and increased reliability. The switch has the following three terminals:

- **Source:** A fixed terminal and supporting anchor for an electrically equivalent, movable cantilever.
- **Gate:** A fixed terminal creating an attracting electrical field to pull in the cantilever when there is a sufficient voltage difference between the source and gate. This voltage difference is defined as the pull-in voltage (V_{pi}).
- **Drain:** A fixed terminal where the cantilever tip makes contact, forming a connection between source and drain when the switch is closed.

The curved design mitigates the excessive field strength towards the edge of the cantilever, typically found in straight cantilever designs [6,20,21]. This improves the margin between V_{pi} and the breakdown voltage, thus increasing robustness. The length of the switch is 5 µm, with a 60 nm air gap between the actuating gate electrode and the cantilever in the open state. When the switch closes, this air gap is approximately half of the initial value.
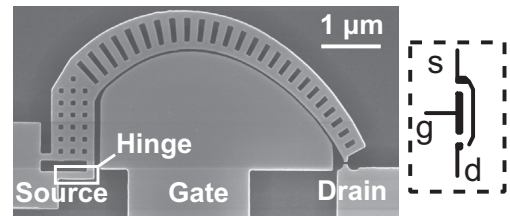

Fig. 1. SEM image of a fabricated curved NEM switch with a hinge length of 0.5 µm (stiff design) and corresponding circuit symbol on the right-hand side.

The design is scalable for smaller feature sizes, where a decreased air gap of 5 nm and a sub-micron device length enable sub-nanosecond switching times and operating voltages below 1 V [4,20].

The conducting coating consists of platinum with gold to reduce structural stress and eliminate out-of-plane bending of the switch. A thin layer of amorphous carbon (a-C) is deposited onto the first layer to benefit from the lower surface energy [21]. Nanoscale contacts are formed in the a-C by applying a sufficiently high voltage in the range of 1.5–2.5 V, allowing current to flow through local filaments without large adhesive forces. This reduces the restoring force of the relay to less than 100 nN and decreases the on–off hysteresis window from over 2 V for a platinum–platinum contact to 0.5 V for the a-C contact [21]. Reliability measurements show that the curved design combined with a-C can operate for over 100 million hot-switching cycles as a standalone switch [21]. After a sufficient number of conduction filaments in the a-C have been formed through repeated hot-switching, the on-resistance (R_{on}) drops to less than 50 kΩ.

For the experiments presented in this paper, we used two NEM switch designs with different hinge lengths. The hinge defines the stiffness and, hence, the V_{pi} of the switch. Finite-element analyses have shown that a hinge of 0.5 µm (stiff switch, Fig. 1) corresponds to a V_{pi} of 10.3 V and an expected mechanical pull-in time of 23 ns, whereas a hinge of 1.0 µm (soft switch) corresponds to a V_{pi} of 7.6 V and an expected mechanical pull-in time of 48 ns.

2.2. Device fabrication

The fabrication of the NEM switch (Fig. 2) involves the use of electron beam lithography on a silicon-on-insulator (SOI) substrate combined with hydrogen-bromide-based inductively coupled plasma (ICP) etching of a 220-nm-thick silicon device layer [21]. During this step, the 60-nm air gap is directly etched as well. Next, the silicon dioxide beneath the device layer is etched with an undercut, creating free-standing structures. The undercut eliminates the formation of electrical shortcuts through the conduction
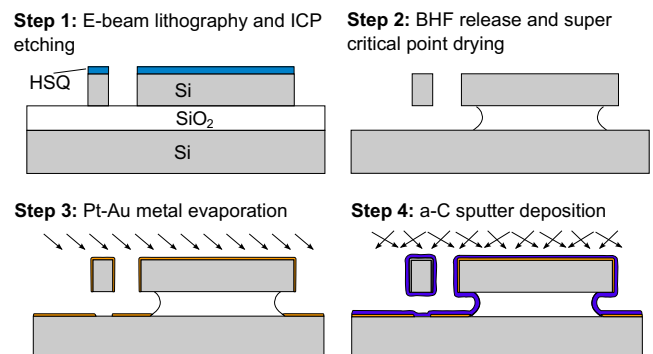

Fig. 2. Fabrication process steps for the curved NEM switch.