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Letter

Superconducting platinum silicide for electron cooling in silicon

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ABSTRACT

We demonstrate electron cooling in silicon using platinum silicide as a superconductor contact to selectively remove the highest energy electrons. The superconducting critical temperature of bulk PtSi is reduced from around 1 K to 0.79 K by using a thin film (10 nm) of PtSi, which enhances cooling performance at lower temperatures. We use an electron cooling model to infer that electrons in silicon are cooled from 100 mK to 50 mK in such a device.

1. Introduction

The Schottky junction between a degenerate semiconductor and a superconductor [1] forms a natural tunnel barrier, which enables this type of superconductor–semiconductor junction to be used as an energy selective filter, removing hot electrons from the semiconductor and replacing them with cold electrons [2]. Such junctions can be useful for electron cooling at low temperatures, especially as the thermal coupling between a crystal lattice and an electron gas therein can become very weak below 1 K [3]. Hence an electron gas within a degenerately doped semiconductor, can be cooled below the lattice temperature with moderate cooling power.

Provided that the electron temperature T_e and lattice temperature T_{ph} (assumed equal to the bath temperature T_b) are sufficiently below the superconducting transition temperature T_C of the superconductor, the cooling power increases with temperature ($T_e^{3/2}$) [2], but at a lower rate than the lattice heat load (typically T_{ph}^5 or T_{ph}^6) [4,5]. So in principle, cooling should improve as temperature is reduced. However, at the lowest temperatures other heat loads may become dominant, such as sub-gap leakage currents or heat received from the surroundings via radiation or conduction [6]. The sub-gap leakage can be reduced by using narrow energy gap superconductors because this reduces the number of states in the superconducting gap that can otherwise reduce the energy filtering efficiency of the tunnel junction (see below).

Silicides have been widely used as contact materials in the semiconductor industry, due to their reliability and good electrical characteristics. Platinum silicide is also known to act as a superconductor with a T_C of about 1 K for bulk PtSi. This T_C value is suppressed in thin films with a layer thickness below about 50 nm [7] which is an indication that the superconducting gap is less in thin films than in the bulk. The thinnest PtSi films can have better crystallinity [7], which results in a smoother interface to the silicon and hence a better junction quality. Motivated by these properties and the compatibility of PtSi with Si we have used a 10 nm thick PtSi film of platinum silicide as the superconductor in a tunnel junction refrigerator for electron cooling in silicon and we report on the outcomes.

2. Experimental

PtSi–Si tunnel junctions were fabricated to form a superconductor – semiconductor – superconductor structure (S-Sm-S). The device cross-section is shown in Fig. 1a. A silicon-on-insulator

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(SOI) substrate was used and the active areas were ion implanted with arsenic, giving a dopant concentration of 8×10^{19} cm^{-3} after activation. Platinum was deposited and silicidation was performed at 500 °C for 1 min. Finally, aluminium contacts were patterned by lift-off. Hall bar current–voltage (I–V) measurements gave a sheet resistance of about 100 Ω/square for the doped Si layer. The sheet resistance and carrier density values agree well with standard curves for silicon [8]. Fig. 1b shows the device in plan-view. The implanted region between the contacts is just over 3 times longer than its width (5 μm), giving a series resistance R_S of 320 Ω.

In Fig. 2 we compare T_C measurements for PtSi films of different thickness on low doped silicon substrates. The T_C is reduced from 1.015 K for the 100 nm film, to 0.786 K in the 10 nm film. This reduction is similar to, but a little less than, previously reported where a T_C of ~0.6 K was obtained for a similar thickness film [7].

I–V measurements were performed on the PtSi device at 100 mK using a dilution refrigerator and are shown with a logarithmic current axis in Fig. 3a. The same data are also shown with a linear current axis (inset) and used to calculate the differential conductance dI/dV (Fig. 3b).

We fitted the I–V data using [9]:

$$I = \frac{1}{2eR_T}\int_{-\infty}^{\infty}\left[f(E-\frac{1}{2}eV_C,T_e)-f\left(E+\frac{1}{2}eV_C,T_e\right)\right]g(E,\Gamma)\,\mathrm{d}E. \quad (1)$$

where T_e is the electron temperature, the Fermi distribution function $f(E,T) = 1/[1 + \exp(E/k_BT)]$, k_B is the Boltzmann constant, e is the electron charge and the Dynes function for the density of states of a superconductor is given by [10]:

$$g(E,\Gamma) = \left|\mathrm{Re}\left[\frac{E+i\Gamma}{\sqrt{(E+i\Gamma)^2-\Delta^2}}\right]\right| \quad (2)$$

The Dynes leakage parameter Γ implies the presence of gap states in the superconductor and is generally used as a figure of merit for superconductor tunnel junctions, with a lower value indicating a better quality junction.

The voltage dropped across the PtSi junctions V_C determines the current and cooling power of the junctions. The model is calculated for a range of values of V_C. The total voltage dropped across the device, for comparison with the measurement, is then calculated

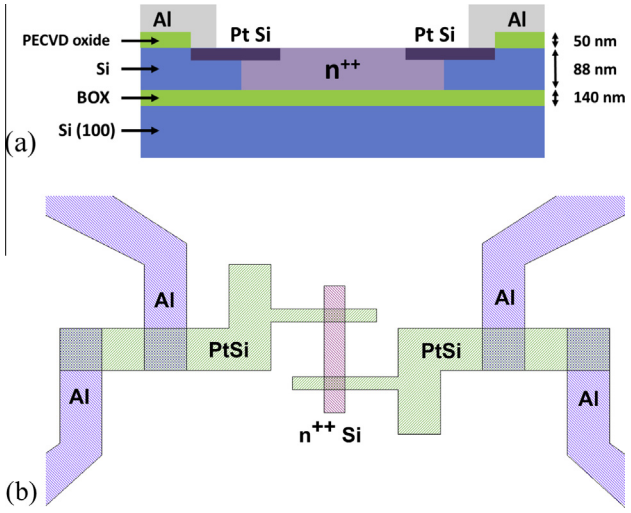

Fig. 1. (a) Schematic cross-section. A silicon-on-insulator substrate was used with a 140 nm buried silicon dioxide layer (BOX). (b) Device layout. The length of the central n++ island is approximately 30 μm and the junction areas are 2.5 μm by 5 μm. The four Al contacts allow a four point measurement, eliminating any voltage drops in the Al–PtSi junctions.

using $V_T = V_C + IR_S$, where R_S is the series resistance of the silicon region. To implement the *cooling model* of Ref. [11] we use an expression for the cooling power of the S-Sm-S junctions.

$$P_c = -\frac{2}{e^2R_T}\int_{-\infty}^{\infty}\left(E-\frac{1}{2}eV_C\right)\left[f\left(E-\frac{1}{2}eV_C,T_e\right)-f(E,T_b)\right]g(E,\Gamma)\mathrm{d}E \quad (3)$$

in a heat balance equation

$$P_C + P_{e-ph} + P_J = 0 \quad (4)$$

to solve for T_e. The heat power input to the electron system from the lattice by electron–phonon coupling is $P_{e-ph} = -\Sigma v(T_e^6 - T_b^6)$, where Σ is the electron–phonon coupling constant, v is the volume of the electron gas and T_b is the bath temperature [12,13]. The only other heat input considered is via Joule heating of $P_J = I^2 R_s$. Joule heating is significant as a result of the series resistance, and Joule heating is about a factor of 10 higher than the lattice heating at the optimum cooling bias (and is approximately 50 fW). However, the temperature dependence of the cooling power is stronger than that of Joule heating at this bias so that cooling is still dominant. With Joule heating removed from the model, the minimum temperature (achieved at slightly higher cooler bias) reduces to about 40 mK. The Joule heating could be reduced to a low level if the device geometry was such that the series resistance region was at least 3× wider than its length.

Initially we consider an *isotherm model* where there is no cooling of the electrons by the junction. Using (1) and (2) with T_e = - T_b = 100 mK we can obtain a reasonable fit to the data outside of the region where electron cooling might be expected, as shown by the dashed red curves in Fig. 3a and b. By fitting this ohmic region we found the tunnel resistance R_T = 300 Ω (3.75 kΩ μm^2), superconductor half-gap Δ = 70 μeV and Dynes leakage parameter $\Gamma\Delta = 8 \times 10^{-3}$. This Dynes value is fairly typical of other semiconductor devices [11], but not as low as that found in normal metal based coolers [6]. From the Bardeen–Cooper–Schrieffer formula ($\Delta = 1.764\ k_B\ T_C$) the superconductor half-gap value extracted would correspond to a T_C of 0.46 K, which is rather smaller than measured in Fig. 2 on a continuous PtSi film. Reasons for the discrepancy could be a result of the device process leading to a thinner than expected PtSi layer in the actual cooler region, the fabrication process degrading the superconducting properties in some way. Nevertheless, the IV curves in Fig. 3 do show a distinct transition at $|V_T| < 0.14$ mV, which is assumed to correspond to a transition from sub-gap to normal state resistance at $|V_T| = 2\Delta/e$ in the cooling model and confirms the parameter Δ = 70 μeV for the particular device being studied.

In Fig. 3b, the calculated isotherm (dashed red curve) falls to the minimum with straight sides on the log-linear plot, which does not agree with the experimental data. This exponential behaviour is typical of an isotherm plot and provides a clear distinction from a device that is cooling [14]. Fig. 3 shows that the isotherm model does not capture the experimental data at lower bias ($|V_T| < 0.1$ - mV). The observation of a reduced current relative to that calculated in the isotherm model is a characteristic sign of cooling in the device [14].

By instead using the value of T_e set by the solution of (4) (*cooling model*) to calculate the current in (1) we are better able to reproduce the experimental I–V curve in the sub-gap region (for bias $|V_C| < 2\Delta/e$) as shown by the solid blue curve in Fig. 3. We used $\Sigma = 3.1 \times 10^8$ W m^{-3} K^{-6} from Kivinen et al. [13] for a similar sample, the volume $v = 32\ \mu\mathrm{m} \times 5\ \mu\mathrm{m} \times 88\ \mathrm{nm} = 1.41 \times 10^{-17}$ m^{-3} and kept the same values of Δ, Γ R_T and R_S used in the isotherm model. The best fit of the cooling model to the experimental data predicts cooling of the electron system from 100 mK to about 50 mK, as shown by the calculation in Fig. 4 (solid blue curve) made using