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Letter

Comparison of electron–phonon and hole–phonon energy loss rates in silicon

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ABSTRACT

The hole-phonon energy loss rate in silicon is measured at phonon temperatures ranging from 300 mK to 700 mK. We demonstrate that it is approximately an order of magnitude higher than the corresponding electron–phonon energy loss rate over an identical temperature range.

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1. Introduction

In the low temperature (sub 1 K) regime, charge carriers are heated only weakly by the crystal lattice due to the strong temperature dependence of the carrier-phonon coupling. However, phonon heating of charge carriers is still a major factor in the heat balance for electron cooling applications [1] and is also responsible for the phonon noise equivalent power, an important parameter for measurement of electromagnetic radiation in astronomical detectors [2]. Previous studies in this field have illustrated the dependence of the electron–phonon coupling on mechanical strain [3]. In this work we have sought to illustrate the effect of carrier type on the carrier-phonon coupling and investigate both hole and electron devices.

Our hole sample consisted of a 30 nm silicon layer with a boron doping concentration of 4×10^{19} cm^{-3} (verified by Hall measurements, see below) grown by reduced pressure chemical vapour deposition (RP-CVD). Replacing the dopant with phosphorus, an otherwise identical sample was grown to serve as our electron control. Aside from this change in dopant type the two samples underwent the same fabrication process in order to allow for a direct comparison between the two. We assume that material quality is similar for both n and p samples, given that both samples were grown in-house on high quality substrate, using the same CVD reactor and using appropriate high purity gasses. The fabrication method is outlined below and is given in detail in Ref. [3]. The device geometry is depicted in Fig. 1. The mesa was patterned by photolithography followed by a plasma etch, leaving a raised rectangular pillar 100 nm tall with dimensions 205 nm by 5 nm. The active layer is confined to the top 30 nm, thus the degenerately doped material is effectively isolated and the mesa geometry well defined. The surface was then cleaned in 1% HF before aluminium was deposited via sputtering and patterned to form contacts at both the ends and the middle of the semiconductor bar.

The semiconductor (silicon) – superconductor (aluminium) junctions formed by this process are well understood [4] and behave in much the same way as a normal metal – insulator – superconductor junction [5,6].

The parameters of the two samples used in this experiment are presented in Table 1, with the mobility, carrier density and sheet resistance deduced from resistivity and Hall measurements carried out at 10 K, where the carrier gas is degenerate and the Hall scattering factor is unity [7]. The sample thickness was obtained from secondary ion mass spectrometry measurements and used to convert sheet carrier density to a volume carrier density.

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Table 1
Sample parameters from Hall measurements made at 10 K.

Sample	Mobility ($cm^2 V^{-1} s^{-1}$)	Carrier density ($10^{19} cm^{-3}$)	Sheet resistance ($\Omega \square^{-1}$)
Hole	68	4.3	354
Electron	192	3.1	350

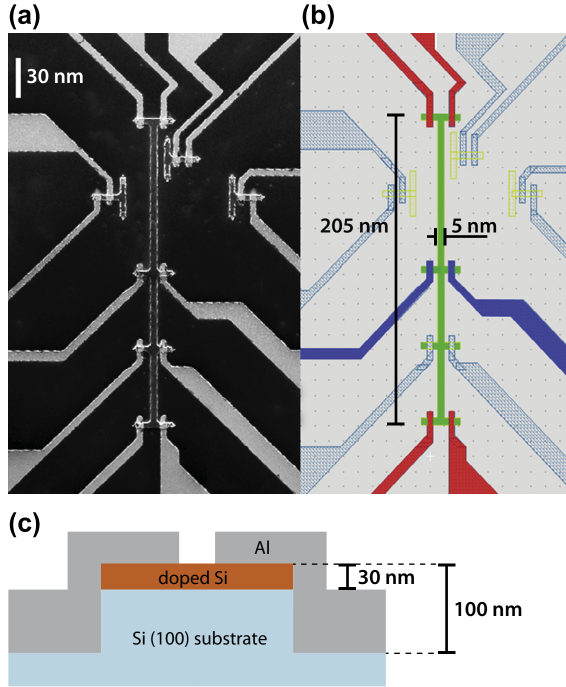

Fig. 1. (a) An SEM micrograph of a carrier-phonon test structure. (b) The device schematic. Aluminium leads for the heating of the bar are shown in red whilst the thermometer leads are coloured blue. Each individual junction has an area of 16 μm^2. The central green area is the highlighted mesa bar structure. (c) A schematic depicting the cross-section of the device and layer thickness. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

The S–Sm–S junctions positioned in the middle of the mesa have a minimal cooling power and are used to measure the electronic temperature (T_e) of the semiconductor bar. At millikelvin temperatures and under conditions $k_B T_e << \Delta$ and $0 << eV < \Delta$, the current through such junctions due to thermally activated tunnelling is given by [8,9]

$$I(V) \approx I_0 exp[(eV - \Delta)/k_B T_e] \quad (1)$$

where $I_0 = (\Delta/eR_n)(\pi k_B T_e/2\Delta)^{1/2}$ and R_n is the normal state resistance.

The junction is biased with a constant current such that the voltage response becomes approximately linearly dependent on electronic temperature, according to

$$\frac{dV}{dT_e} \approx \frac{k_B}{e} \ln\left(\frac{I}{I_0}\right) \quad (2)$$

The bias current is selected to provide the maximum voltage response to a change in temperature whilst having only a minimal heating effect on the bar itself.

Figs. 2 and 3 show the current voltage behavior of the thermometer junctions at high and low temperature. It can be seen that the optimum current corresponding to the widest voltage range between the two temperature extremes is between 10 and 100 nA. For this experiment we use the lowest value in this range.

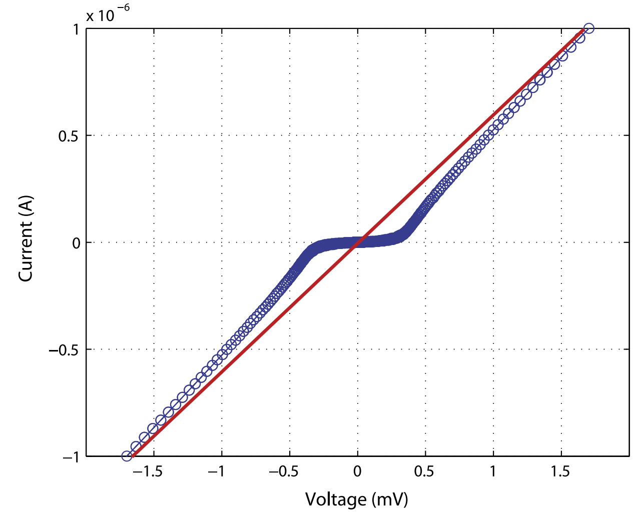

Fig. 2. Current voltage measurements of the S–Sm–S thermometer on our n-doped sample. 300 mK data is shown in blue and room temperature data in red. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

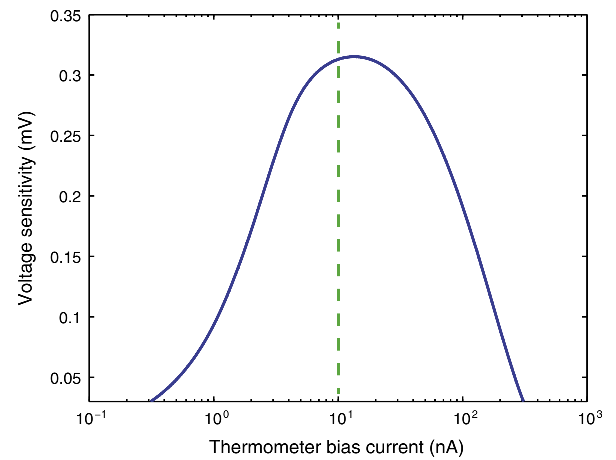

Fig. 3. A plot of thermometer bias current versus the maximum change in thermometer voltage across the entire range of operational temperatures. This enables the identification of the optimum current. The bias used in this experiment is marked by the green dashed line. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

The current bias must be isolated from the varying heating current supplied to the bar. To this end a pair of lock-in amplifiers was used in the configuration shown in Fig. 4. The signal from lock-in 1 was capacitively coupled to the thermometer so as not to disturb its dc bias. To enable this, the ac signal was applied to one contact and its inverse (180° out of phase) to the other. The resulting differential bias, balanced across the thermometer is in phase with this signal and double its amplitude. Lock-in 1 is used to measure the voltage across the thermometer whilst the magnitude of the bias current is monitored by lock-in 2, synchronised to the signal generated by lock-in 1.

The small junction thermometers are calibrated against a conventional ruthenium oxide thermometer mounted in the cryostat, with the uncertainty in this calibration (~2%) being the dominant source of error in our measurement. Starting at a set bath temperature (T_B), a variable current bias is applied to inject a range of heating powers through the semiconductor bar which act to heat the charge carriers above the local phonon temperature. The

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